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COA University Questions

May 2015

- 1. Simplify Following $F(A,B,C,D)=\sum m(1,7,10,13,14)+d(0,5,8,15)$
- 2. Compare DRAM and SRAM
- 3. Write short notes on half adder. Draw circuit diagram.
- 4. What is a latch? Explain all its properties. Also explain S-R FF.
- 5. Discuss set associative mapping structure in cache memory.
- 6. Explain bus interconnection structure
- 7. What is RAID? Explain any four RAID levels.
- 8. Explain DMA method of I/O with suitable diagram.
- 9. Explain different addressing modes along with the address calculation formula and advantages and disadvantages of the same with example.
- 10. Discuss superscalar processors and the instruction issues policies used in them.
- 11. Explain sequences of micro operation for various addressing modes in control unit.
- 12. Explain the concept of cloud computing.
- 13. Discuss bus design elements
- 14. Discuss a 4 bit synchronous counter.
- 15. Write Short note:
 - a) Clusters
 - b) Associative Memory
 - c) Multiplexer and De-multiplexer
 - d) Micro programmed control

DEC 2014

- 1. Differentiate between superscalar and super pipelined approaches.
- 2. Simplify the Boolean functions
 - i. $F(A,B,C,D)=\sum (0,1,3,4,8,10,11,12,14)+d(5,9)$
 - ii. $F(A,B,C,D)=\pi(2,5,7,8,9,10,12)$

Also draw the circuit diagram of the simplified equation using minimum number of gates

- 3. Explain full adder with logic diagram.
- 4. Define flip flop. Explain the working of J-K FF with logic diagram.
- 5. Explain Flynn's classification with diagrams.
- 6. Define associative memory. Explain its working.
- 7. Define Cache memory. Explain any two cache memory mapping in detail
- 8. List and briefly define types of super scaler instruction issues policies.
- 9. Explain control signal generation using micro programmed control. Draw necessary diagram.
- 10. Explain fetch cycle, indirect cycle and interrupt cycle. Show the flow of data during each cycle using suitable diagram.
- 11. Discuss the functions of I/O module. Explain interrupt- driven and DMA technique in details.
- 12. With a circuit diagram explain a 4 bit ripple binary counter.
- 13. Define cluster explain different clustering methods in detail with its benefits and limitations
- 14. What is RAID? Explain any 3 RAID level in detail with suitable diagrams.
- 15. Explain system bus. Write different bus arbitration methods
- 16. List and explain different addressing modes with suitable examples.

May 2014

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- 1. Draw the typical DMA block diagram
- 2. Compare micro programmed control unit VS hardware control unit
- 3. Using K-Map simplify the following expression in four variable A,B,C,D. $F(A,B,C,D)=\sum(0,2,4,5,6,7,8)+d(12,13,14,15)$.
- 4. What do you mean by counter? Explain types of counters?
- 5. What do you mean by RAID? Explain any four RAID levels.
- 6. List and explain the use of general purpose register in CPU.
- 7. Discuss the superscalar processor and the instruction issues policies used in them.
- 8. Explain memory hierarchy. What is cache memory? Why it is used?
- 9. What is PROM, EPROM and EEPROM? Differentiate between static RAM and dynamic RAM.
- 10. Explain the symmetric multiprocessor and their organization.
- 11. Draw the diagram of flynn's classification of parallel processing.
- 12. Explain the working of half adder.
- 13. Draw the diagram of I/O module.
- 14. What is bus arbitration? Explain daisy chaining and polling with suitable block diagrams.
- 15. Explain hardwired implementation of control unit with diagram.
- 16. Write a note on six stage instruction pipelining and effect of conditional branches on the same operation
- 17. Explain the concept of cloud computing.

Dec 2013

- 1. Draw the block diagram of an I/O module.
- 2. Compare sequential Vs combinational circuit.
- 3. Using K-Map simplify the following expression in four variable K, L, M, N. $F(K,L,M,N)=\sum(1,7,10,13,14)+d(0,5,8,15)$.
- 4. Discuss 3-to-8 decoder using truth table. Draw its implementation using the appropriate gates
- 5. Discuss the set associative cache organization with an example.
- 6. Discuss SMP organization in detail.
- 7. Explain different addressing modes along with the address calculation formula and advantages and disadvantages of the same.
- 8. What is interrupts? Explain a complete instruction cycle state diagram with interrupts.
- 9. Discuss the 4bit synchronous counter.
- 10. Explain the DMA method of I/O technique.
- 11. Differentiate between DRAM and SRAM.
- 12. Draw and explain the block diagram of control unit.
- 13. Design a combinational logic circuit with four input variable that will produce logic 1 output when the number of 1s in the input is even.
- 14. Discuss bus design elements
- 15. Explain the concept of cloud computing.
- **16.** Explain the instruction pipelining in details.
- 17. What do you mean by RAID? Explain any four RAID levels

May 13

- 1. What is FF? Explain working of an A2 J-K FF. Explain all its states.
- 2. Using K-map, simplify the following Boolean function. F(A,B,C,D)=Z(0,1,2,5,8,9,10).
- 3. Design 8—to-1 Multiplex.
- 4. Compare sequential Vs Combination circuits

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- 5. Explain RISC and CISC architectures in detail.
- 6. Explain six stage instruction pipeline. Explain the effect of conditional branching with suitable timing diagrams
- 7. Explain in detail about instruction cycle state diagram.
- 8. What is addressing model'. Explain its types in detail.
- 9. What is cache memory? Explain about associative and set associative mapping of cache.
- 10. Differentiate between the following
 - a. SRAM vs DRAM
 - b. RISC Vs CISC
- 11. Explain different RAID levels in details
- 12. Explain about various I/O transfer techniques
- 13. Explain about the Flynn's classification of SMPs with suitable diagrams
- 14. Explain with diagram the working of a 4 bit Synchronous binary counter.
- 15. Explain in detail about the different superscalar instruction issue policies.
- 16. Explain the following (Any two)
 - i. Micro-Programmed and Hardwired control
 - ii. Decoder(3x8)
 - iii. Full—adder circuit(with truth table)
 - iv. I/O module

DEC 2012

- 1. Write short notes on half adder. Draw circuit diagram.
- 2. Using K-map simplify the following expression in four variable A, B, C, D. $F(A,B,C,D)=\sum m(1,3,5,8,9,11,15)+d(2,13)$.
- 3. Design a combinational logic circuit with three input variable that will produce logic 1 output when more than one input variables and logic 1.
- 4. Convert the following:
 - i. $(66.38)_{10} = ()_8$
 - ii. $(100110111)_2 = ()_{10}$
- 5. Discuss different bus design elements.
- 6. Explain the register organization of CPU.
- 7. Discuss the set associative Cache organization with example.
- 8. Explain the concept of micro programmed control unit.
- 9. Compare SRAM Vs DRAW.
- 10. Draw and explain the Block diagram of I/O module.
- 11. Explain the difference combinational circuit and sequential circuits.
- 12. Explain how branches are handled in instruction pipelining.
- 13. Discuss the concept of clustering in parallel organization
- 14. Explain indirect address, register indirect addressing and displacement addressing with address calculation formula and its advantages and disadvantages
- 15. Discuss the limitation of superscalar organization.
- 16. Explain the concept of cloud computing.
- 17. Write a short note on memory characteristics

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DEC 13 old

- 1. What is FF? Explain working of SR and J-K FF. Explain all its states.
- 2. Compare sequential VA combinational circuits. Discuss 8 to 1 mux using truth table. Draw its implementation using appropriate gates.
- 3. Explain DMA method of I/O technique with suitable diagram.
- 4. Explain six stages instruction pipelines along with conditional branching with suitable timing diagrams
- 5. Compare following:-
 - i. SRAM Vs DRAM
 - ii. Micro Program Vs hardwired control.
- 6. Explain RISC and CISE architecture in detail.
- 7. What is I/O module? Discuss with the help of diagram functioning of I/O module.
- 8. What is cache memory? Explain cache coherence strategies in single and multiprocessor systems.
- 9. Explain different RAID levels in details
- 10. List and explain different superscalar instruction issue policies.
- 11. Define system bus. What is bus arbitration? Explain different methods of bus arbitration with suitable diagrams.
- 12. Explain Flynn's classification with suitable diagrams. Also comment on design issues of pipeline architecture.
- 13. Write short notes on (any four):-
 - a. Memory hierarchy.
 - b. Clusters in parallel organization.
 - c. Associative memory.
 - d. Loop buffer.
 - e. Processor organization.

