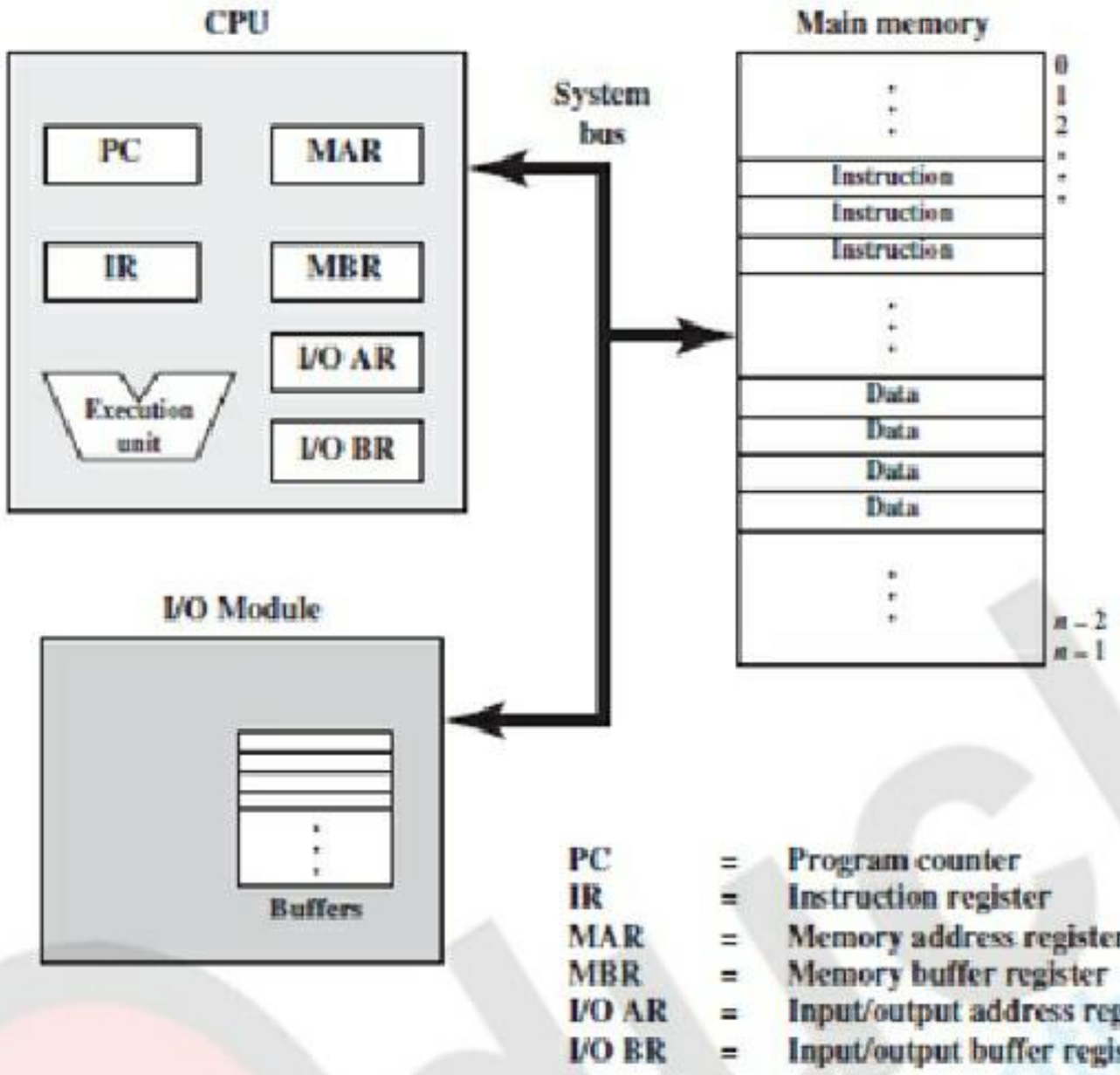
Q.1 COMPUTER COMPONENT-

There are three basic component of computer system that are as follows-



Central processing unit (CPU): Controls the operation of the computer and performs its data processing. That contain following unit-

PC- Program Counter- count the address of next instruction which is to be fetched from memory.

IR- Instruction Register- Contain the instruction.

Execution Unit- Perform the operation and calculation as instructed by computer.

MAR- Memory address register-Specifies the address of memory.

MBR- Memory Buffer register-It contains the copy of designated memory location specifies by memory address register.

I/O AR-specifies the address of I/O operation

I/O BR- Stores the input output operation

Main memory: Stores data.

I/O Module-Moves data between the computer and its external environment.

This above all are the component of computer.

Q.2 Computer Function-

Basic function that computer perform in generally are only four-

1. Data processing
2. Data store
3. Data movement
4. Control

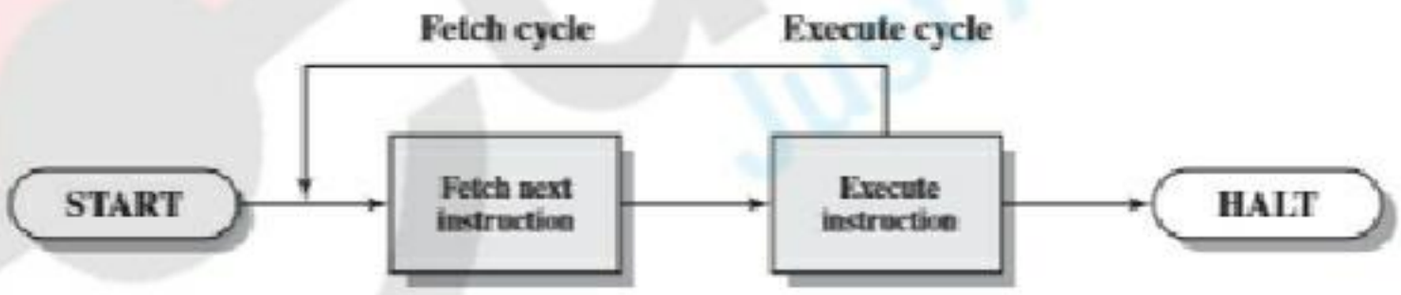
Data Processing-Data processing is the process of gathering and manipulating data,

Data Store- data store are used for storing and managing the data which are process by data processing function.

Data movement- Computer can able to move the data from one device to another device. The movement of data from one peripheral device to other device are also called data communication.

Control-for controlling over all the process control function are used.

Q.3 Explain basic Instruction cycle diagram



If processor fetch one instruction at that time for reducing processor work instruction cycle fetch the next instruction.

Instruction cycle referred to as the Fetch Cycle and Execute Cycle.

At the beginning of each instruction cycle the processor fetches an instruction from memory.

The program counter holds the address of the instruction to be fetched, processor always increment pc so that it will fetch the next instruction in sequence.

In execution of instruction they involved 4 categories

1. **Processor memory**-In this data transfer from processor to memory or from memory to processor
2. **Processor I/o**- In this data can be transferred between two devices.
3. **Data processing**- processor may perform some arithmetic or logical operation.
4. **Control**-instruction specify the sequence of execution.

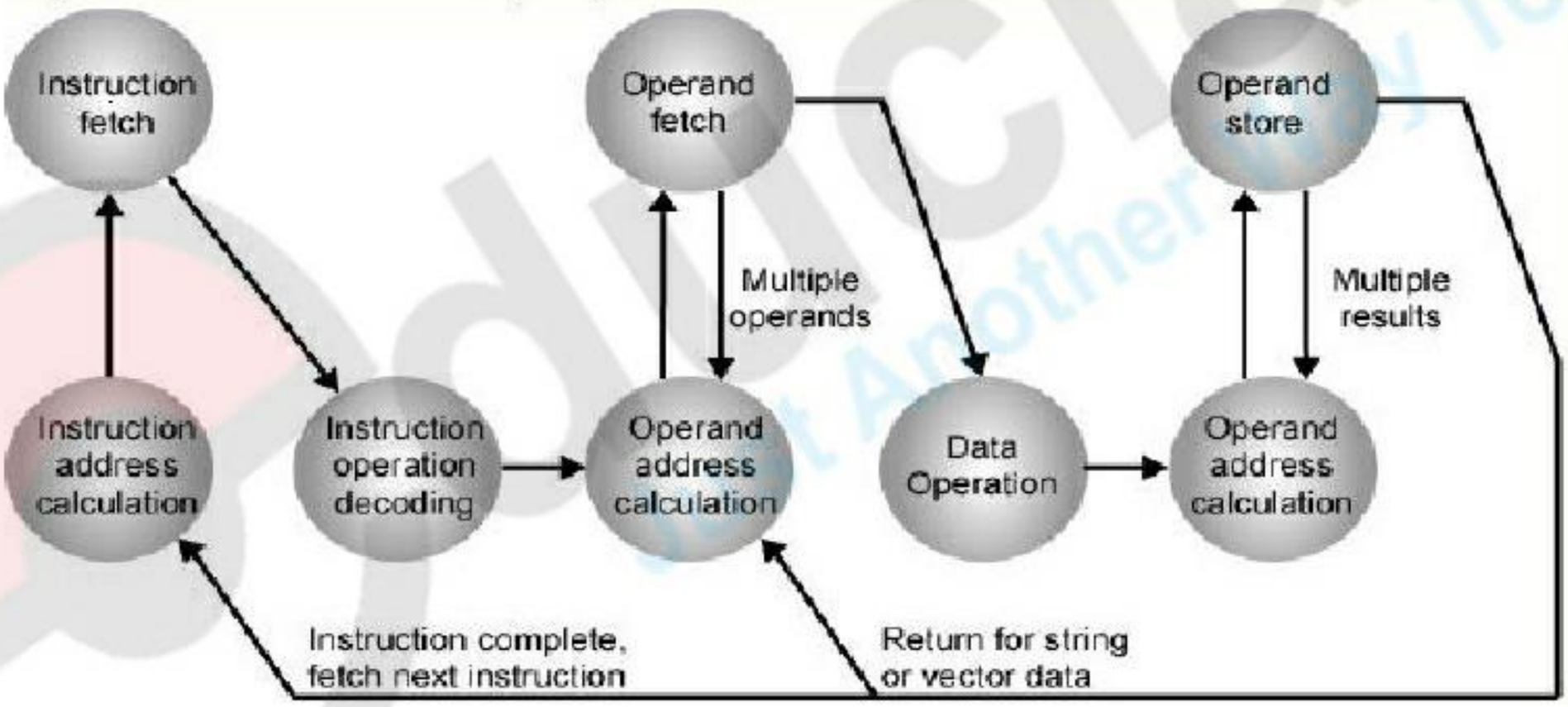
Execution of instruction is combine of this 4 categories.

Program instruction halts only if the system turn off or some error my come.

Q.4 Explain Instruction Cycle State Diagram

Instruction cycle state diagram perform the following function which are related to each other.

The process which are involved in instruction cycle are as follows-



Instruction Address Calculation- determine the address of the next instruction to be executed.

Instruction fetch- Read instruction from its memory location.

Instruction operation Decoding- analyze instruction to determine type of operation to be performed.

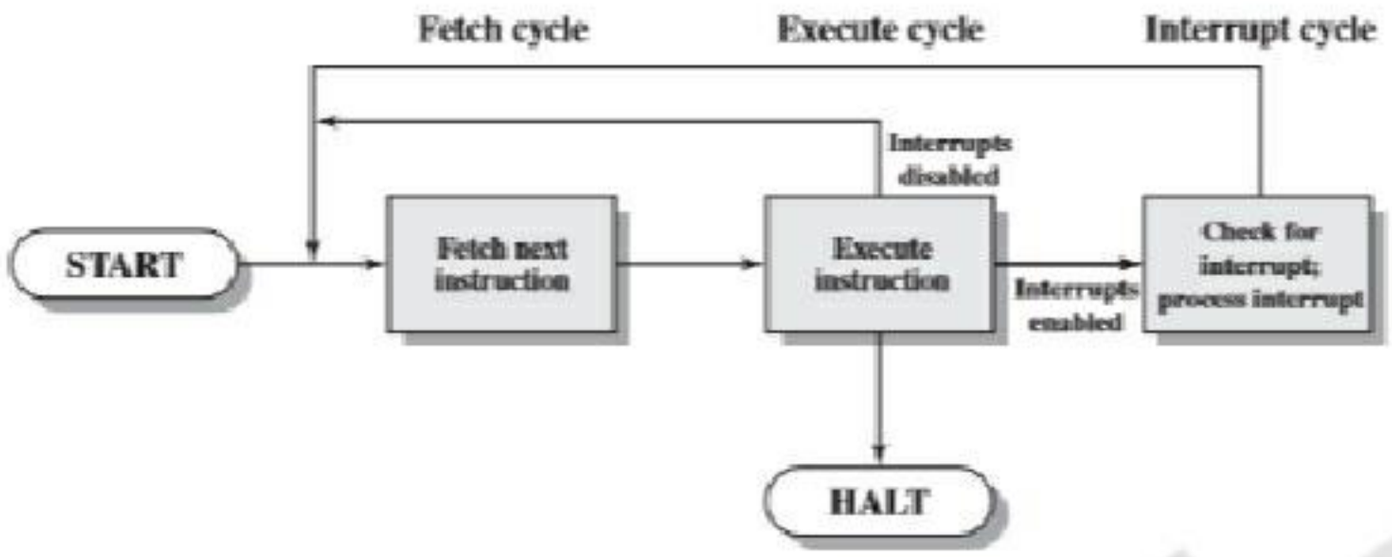
Operand address calculation- determine the address of the operand.

Operand Fetch- Fetch the operand from memory.

Data Operation- Perform the operation indicated in the instruction.

Operand Store-Write the result into memory.

Q.5 Instruction Cycle with Interrupt-



Instruction cycle with Interrupt referred to as the Fetch Cycle and Execute Cycle and interrupt cycle.

At the beginning of each instruction cycle the processor fetches an instruction from memory.

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In execution of instruction they involved 4 categories

1. **Processor memory**-In this data transfer from processor to memory or from memory to processor
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4. **Control**-instruction specify the sequence of execution.

Execution of instruction is combine of this 4 categories.

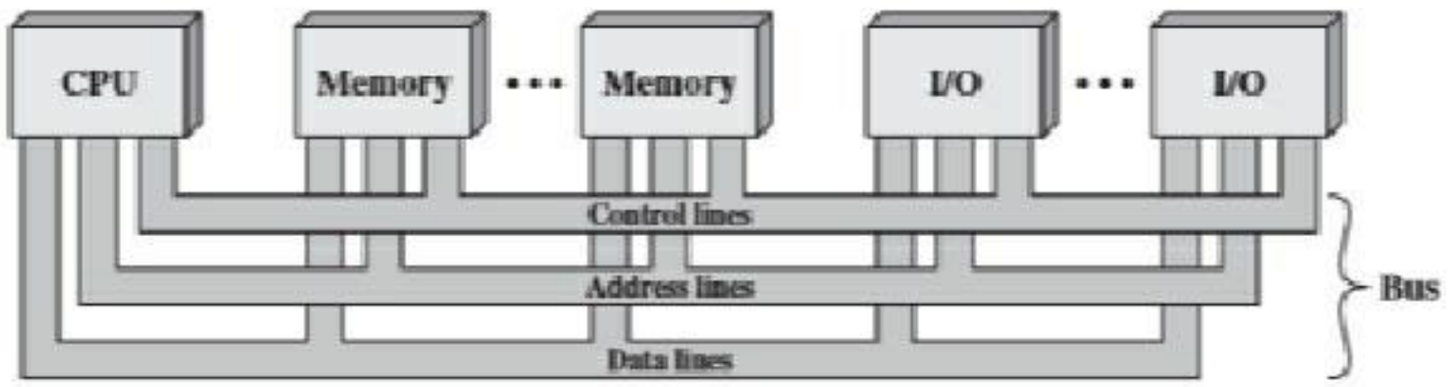
Interrupt Cycle processor check for interrupt. If there is no interrupt fetch the instruction for current program. And if interrupt is pending the suspend the execution of program and interrupt handler come in place.

Program instruction halts only if the system turn off or some error my come.

Q.6 Bus Interconnection Structure

Bus is a communication pathway connecting two or more device.

Following diagram shows the structure of bus



Any bus line can be classified into three functional groups that are DATA, ADDRESS and CONTROL

DATA LINE- providing a path for moving the data among system module. This is also called the DATA BUS.

ADDRESS LINE- Address line are used for transferring a data from source to destination through the data bus.

CONTROL BUS-control bus are used to control the access. Typical control line include memory read, memory write, I/O read, I/O write etc.

Q.7 Elements of bus

Type	**Bus Width**
Dedicated	Address
Multiplexed	Data
Method of Arbitration	**Data Transfer Type**
Centralized	Read
Distributed	Write
Timing	Read-modify-write
Synchronous	Read-after-write
Asynchronous	Block

Type-

Bus type can be classified into two parts-

1. **Dedicated**
2. **Multiplexed**

Dedicated-

Dedicated bus line is permanently assign to one function or physical subset of computer.

Multiplexed-

The method of using same line for multiple process is known as multiplexing.

Method of arbitration-

1. Centralized

2. Distributed

Centralized- In centralized single hardware is responsible for allocating time on bus. This single hardware referred to as a bus controller.

Distributed-

In this process there is no central controller. Each module contain there control logic unit.

Timing-

Synchronous

Asynchronous

Synchronous- occurrence of event on bus is determine by clock.

Asynchronous- occurrence of event on bus follows and depend on the occurrence of previous event.

Bus Width-

Data

Address

Data- The wider data bus, the greater number of bit transferred at one time.

Address-The wider address bus, the greater range of location that can be referenced.

Data Transfer Type-

Read

Write

Read Modify Write

Read After Write

Block Data Transfer

Q.8 RAID-

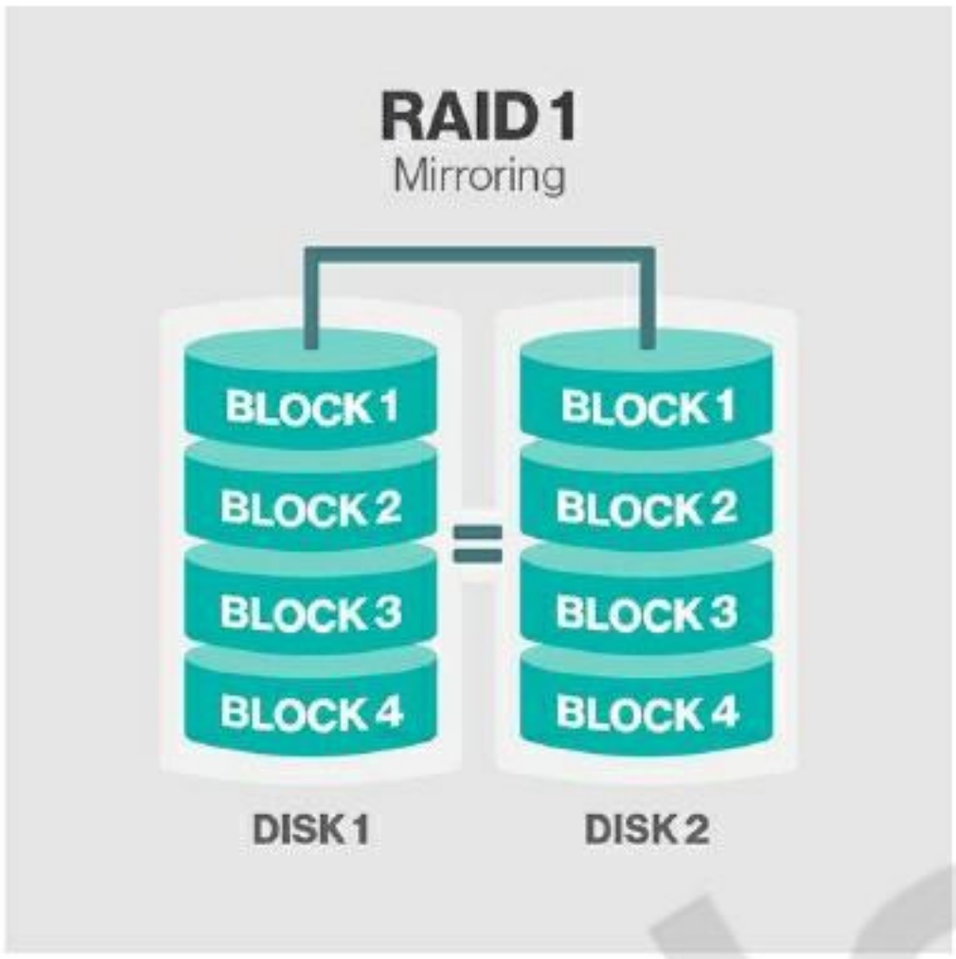
RAID (redundant array of independent disks; originally redundant array of inexpensive disks)

Is a way of storing the same data in different places on multiple hard disks to protect data in the case of a drive failure.

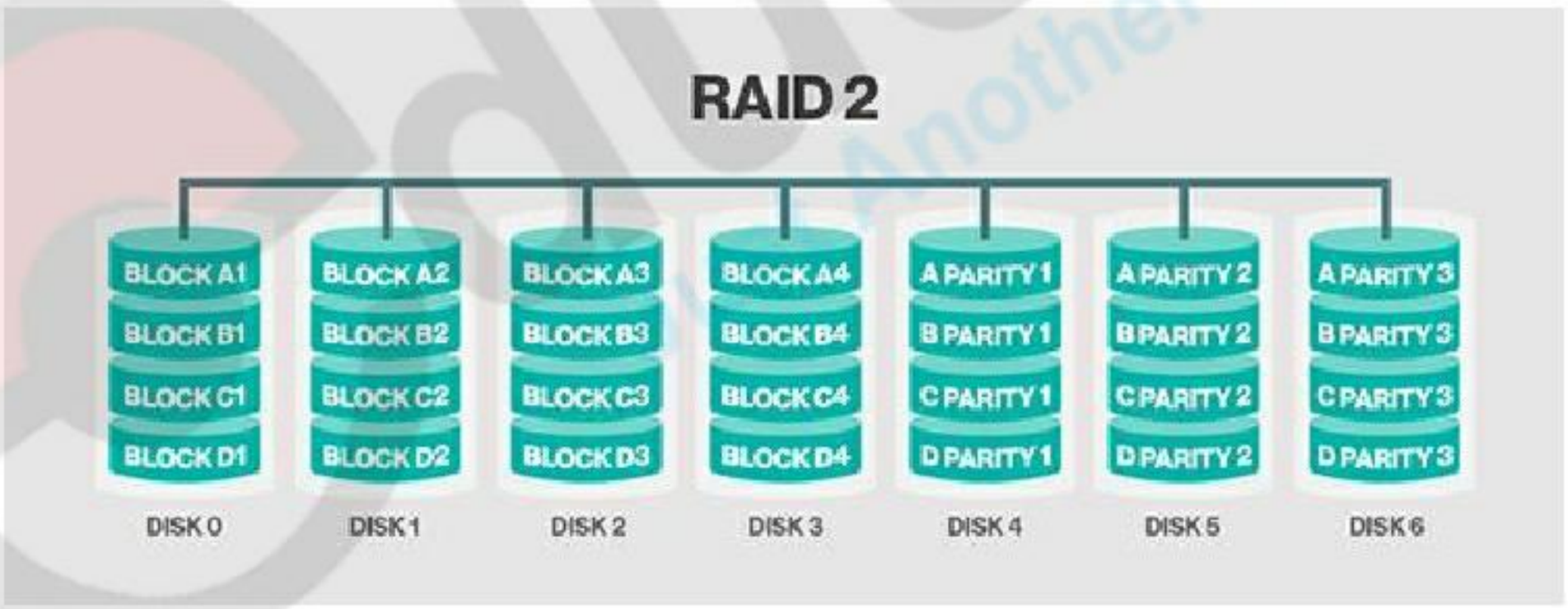
Standard RAID levels

RAID 0: This configuration has striping, but no redundancy of data. It offers the best performance, but no fault tolerance.

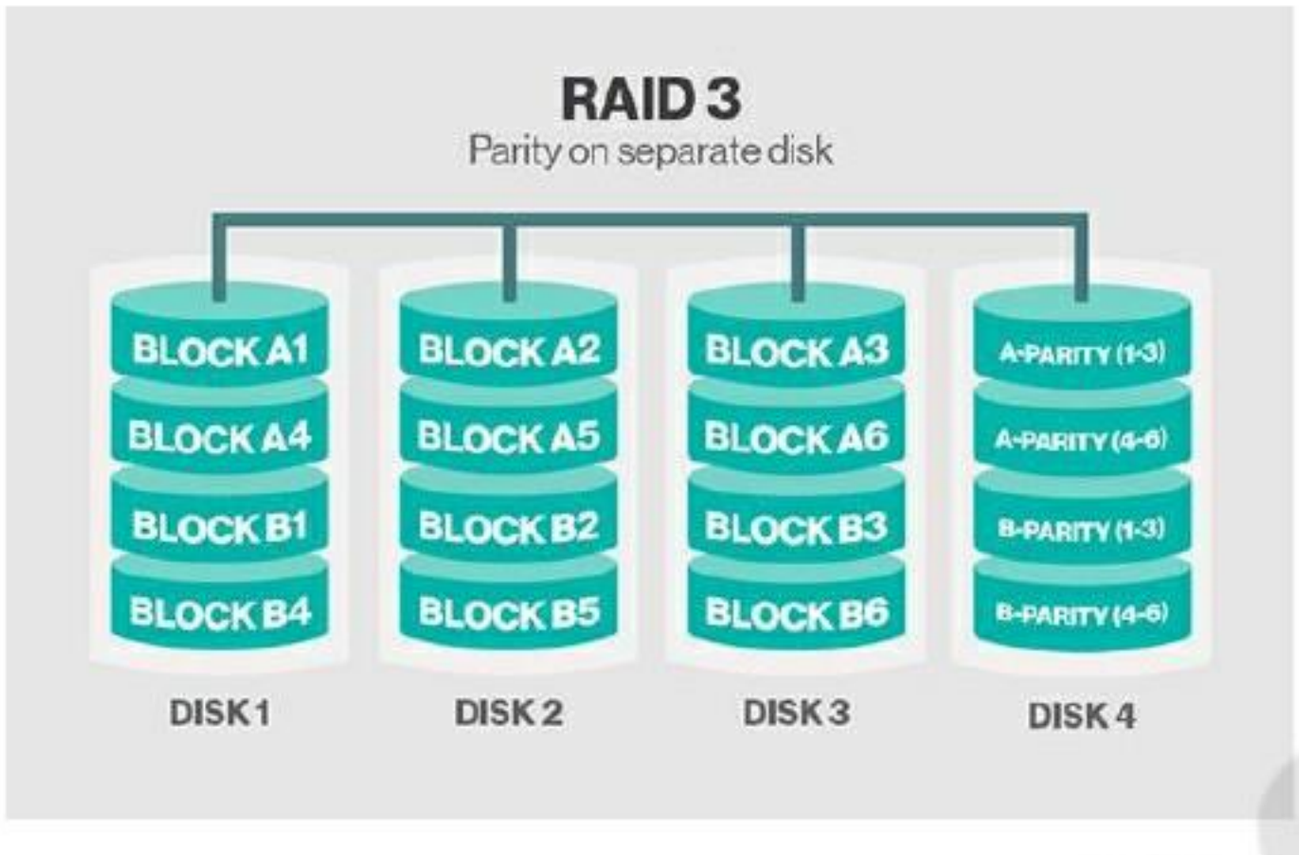
RAID 1: Also known as *disk mirroring*, this configuration consists of at least two drives that duplicate the storage of data. There is no striping. Read performance is improved since either disk can be read at the same time. Write performance is the same as for single disk storage.



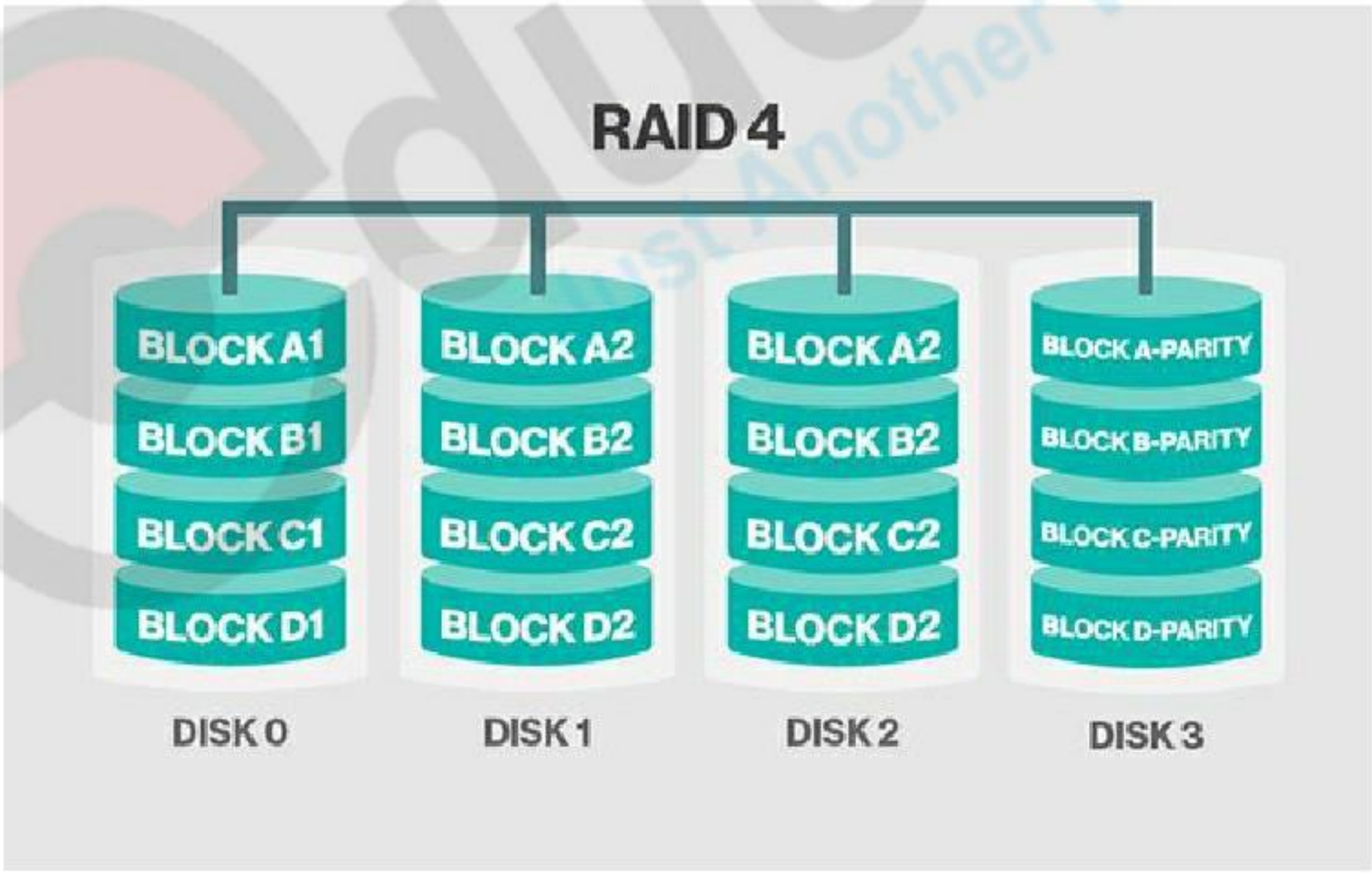
RAID 2: This configuration uses striping across disks, with some disks storing error checking and correcting (ECC) information. It has no advantage over RAID 3 and is no longer used.



RAID 3: This technique uses striping and dedicates one drive to storing parity information. The embedded ECC information is used to detect errors. Data recovery is accomplished by calculating the exclusive OR (XOR) of the information recorded on the other drives. Since an I/O operation addresses all the drives at the same time, RAID 3 cannot overlap I/O. For this reason, RAID 3 is best for single-user systems with long record applications.

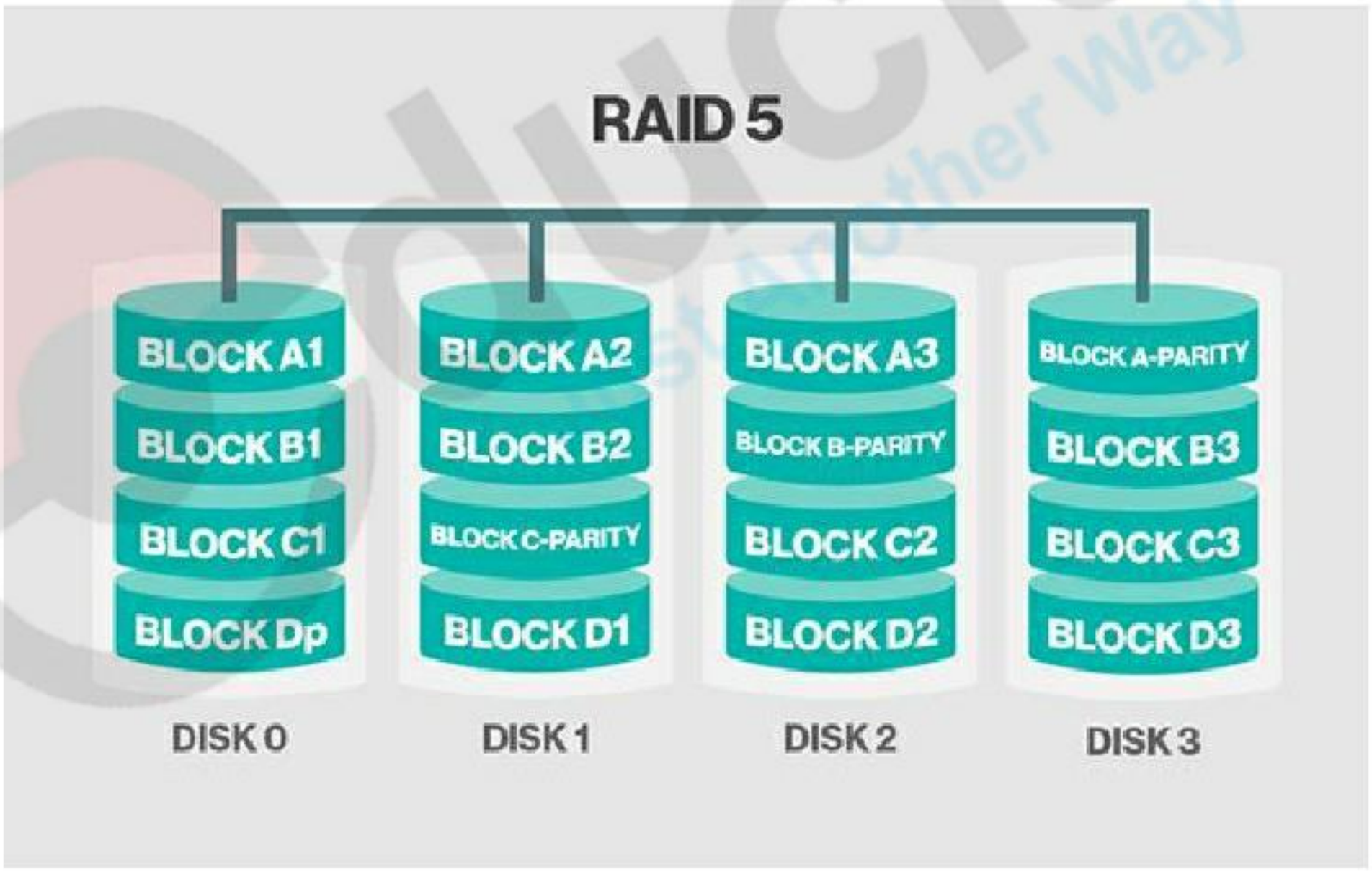


RAID 4: This level uses large stripes, which means you can read records from any single drive. This allows you to use overlapped I/O for read operations. Since all write operations have to update the parity drive, no I/O overlapping is possible. RAID 4 offers no advantage over RAID 5.



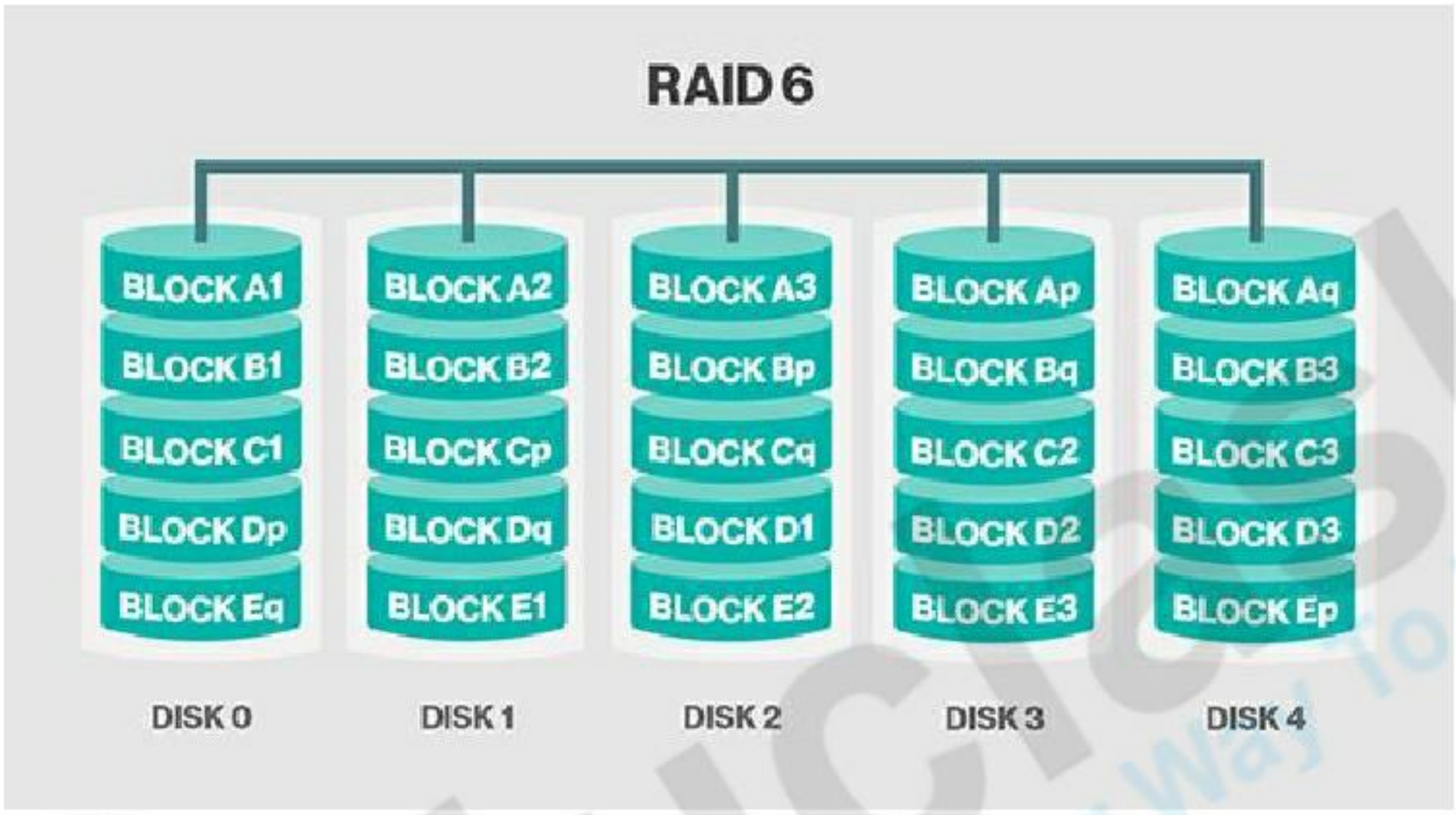
RAID 5: This level is based on block-level striping with parity. The parity information is striped across each drive, allowing the array to function even if one drive were to fail. The array's architecture allows read and write operations to span multiple drives. This results in performance that is usually better than that of a single drive, but not as high as that of a RAID 0 array. RAID 5 requires at least three disks, but it is often recommended to use at least five disks for performance reasons.

RAID 5 arrays are generally considered to be a poor choice for use on write-intensive systems because of the performance impact associated with writing parity information. When a disk does fail, it can take a long time to rebuild a RAID 5 array. Performance is usually degraded during the rebuild time, and the array is vulnerable to an additional disk failure until the rebuild is complete.



RAID 6: This technique is similar to RAID 5, but includes a second parity scheme that is distributed across the drives in the array. The use of additional parity allows the array to continue to function even if two disks fail simultaneously. However,

this extra protection comes at a cost. RAID 6 arrays have a higher cost per gigabyte (GB) and often have slower write performance than RAID 5 arrays.



Q.9 Difference

CISC	RISC
1) CISC architecture gives more importance to hardware	1) RISC architecture gives more importance to Software
2) Complex instructions.	2) Reduced instructions.
3) It access memory directly	3) It requires registers.
4) Coding in CISC processor is simple.	4) Coding in RISC processor requires more number of lines.
5) As it consists of complex instructions, it take multiple cycles to execute.	5) It consists of simple instructions that take single cycle to execute.
6) Complexity lies in microporgram	6) Complexity lies in compiler.

SRAM	DRAM
Stores data till the power is supplied	Stores data only for few milliseconds even when power is supplied
Uses an arry of 6 transistors for each memory cell	Uses a single transistor and capaitor for each memory cell
Does not refreshes the memory Cell	Needs to refresh the memory cell after each reading of the capacitor
Data access is faster	Data acces is slower
Consume more power	Consume less power
Low density/less memory per chip	High density/more memory per chip
Cost per bit is high	Cost per bit is low

Synchronous Counter	**Asynchronous Counter**
All flip flops are triggered with same clock.	Different clock is applied to different flip flops.
It is faster.	It is lower
Design is complex.	I Design is relatively easy.
Decoding errors not present.	Decoding errors present.
Any required sequence can be designed	Only fixed sequence can be designed.

Cache memory

- If the active portions of the program and data are placed in a fast small memory, the average memory access time can be reduced,
- Thus reducing the total execution time of the program
- Such a fast small memory is referred to as cache memory
- The cache is the fastest component in the memory hierarchy and approaches the speed of CPU component

Cache memory cont.....

- When CPU needs to access memory, the cache is examined
- If the word is found in the cache, it is read from the fast memory
- If the word addressed by the CPU is not found in the cache, the main memory is accessed to read the word
- The basic characteristic of cache memory is its fast access time,
- Therefore, very little or no time must be wasted when searching the words in the cache

L1 ,L2 and L3 cache

- L1 cache (2KB - 64KB)
- L1 cache (also known as primary cache or Level 1 cache) is the top most cache in the hierarchy of cache levels of a CPU. It is the fastest cache in the hierarchy. It has a smaller size and a smaller delay (zero wait-state) because it is usually built in to the chip. SRAM (Static Random Access Memory) is used for the implementation of L1.

- L2 cache (256KB - 512KB)
- L2 cache (also known as secondary cache or Level 2 cache) is the cache that is next to L1 in the cache hierarchy. L2 is usually accessed only if the data looking for is not found in L1. L2 is typically implemented using a DRAM (Dynamic Random Access Memory). Most times, L2 is soldered on to the motherboard very close to the chip (but not on the chip itself), but some processors like Pentium Pro deviated from this standard
- L3 cache (1MB -8MB)
- Level 3 Cache - With each cache miss, it proceeds to the next level cache. This is the largest among the all the cache, even though it is slower, its still faster than the RAM.