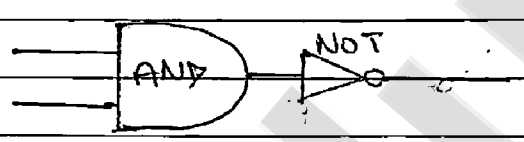
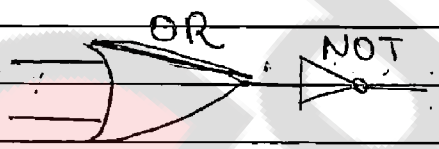
Q) Why NAND and NOR gates are termed as Universal gates?

NAND and NOR Gates are called Universal Gates because all the other gates can be crea-

ted by using these gates Eg:-
NOR as NOT:- This is made by joining the inputs of a NOR gate. As a NOR gate is equivalent to an OR gate leading to NOT gate, this automatically sets to the "OR" part of the NOR gate, eliminating it from consideration and leaving only the NOT part.
NOR As OR :- The OR gate is simply a NOR gate followed by a NOT gate. NOR as AND :- An AND gate gives a 1 output when both inputs are 1, ~~but~~ a NOR gate gives a 1 output only when both inputs are 0. ∴ an AND gate is made by inverting the inputs to a NOR gate. NOR as NAND :- A NAND gate is made by using an AND gate in series with a NOT gate.



= NAND



= NOR

Q2) KMAP

Steps to solve expression using K-map

1) Select K-map according to the number of variables.
2) Identify minterms or maxterms as given in the problem
3) For SOP put 1's in block's of K-map respective to the minterms (0's elsewhere).

4) For POS put 0's in blocks of K-map's respective to the maxterms (& 1's elsewhere).
5) Make rectangular groups containing total terms in power of two like 2, 4, 8 (except 1) and try to cover as many elements as you can in one group.
6) From the groups made in step 5 find the product terms and sum them up for SOP form.

SOP form

K-map for 4 variables

$F(P, Q, R, S) = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$

RS \ PQ	00	01	11	10
00	1 (0)	(4)	(12)	1 (8)
01	(1)	1 (5)	1 (13)	(9)
11	(3)	1 (7)	1 (15)	(11)
10	1 (2)	(6)	(14)	1 (10)

$QS + Q'S'$

POS form

$F(A, B, C, D) = \Pi(3, 5, 7, 8, 10, 11, 12, 13)$

CD \ AB	00	01	11	10
00	1 (0)	1 (4)	0 (12)	0 (8)
01	1 (1)	0 (5)	0 (13)	1 (9)
11	0 (3)	0 (7)	1 (15)	0 (11)
10	1 (2)	1 (6)	1 (14)	0 (10)

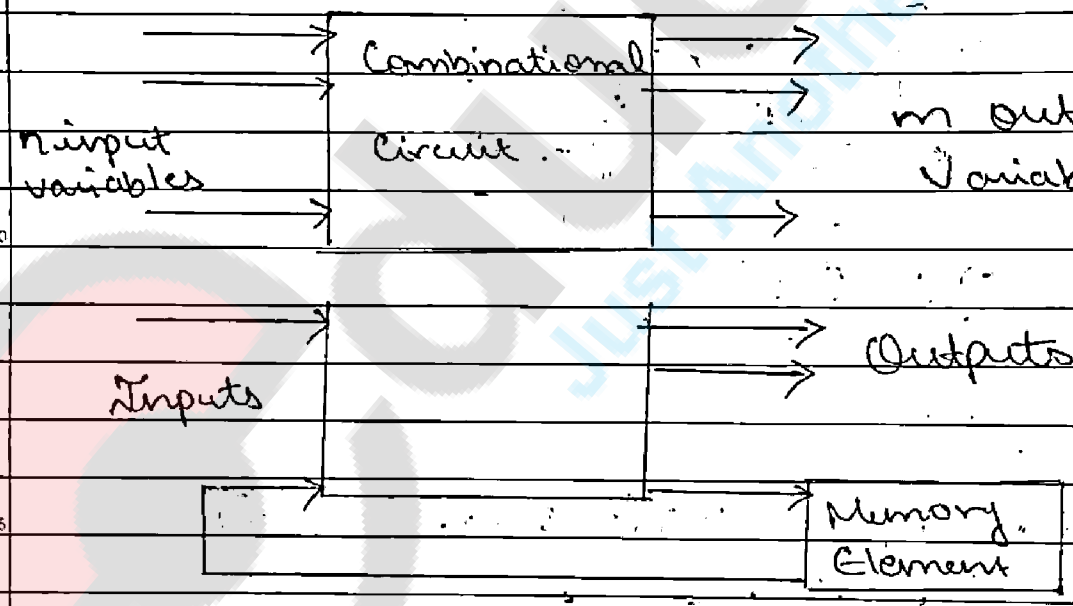
$(A\bar{C}\bar{D}) \cdot (C + \bar{D} + \bar{B}) \cdot (\bar{A} + C + D) \cdot (\bar{A} + B + \bar{C})$

Q3) Compare combinational and sequential circuits

Any circuit can be configured under either sequential or combinational circuit.

Combinational circuit :- Output of combinational circuit depends purely upon PRESENT input, hence it doesn't require memory to store past inputs (preceding inputs).

Sequential circuit :- Sequential circuit requires Memory element, because its output depends upon present as well as preceding inputs. Basically Sequential circuit is combination of Memory element and combinational circuit.



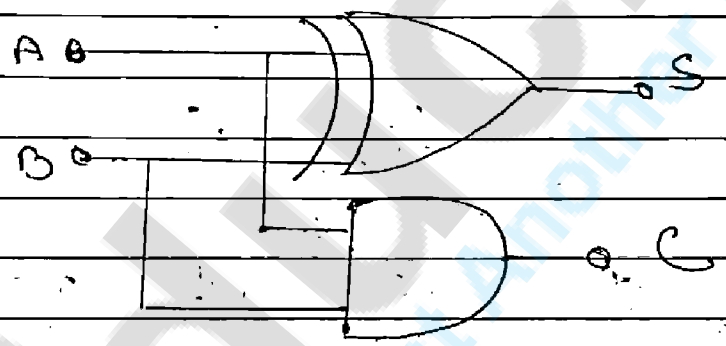
Q4) Half adder :- A half adder is a type of adder that performs addition of numbers. The half adder is able to add two single binary ~~numbers~~ digits and provide the output plus a carry value.

It has 2 inputs called A and B and

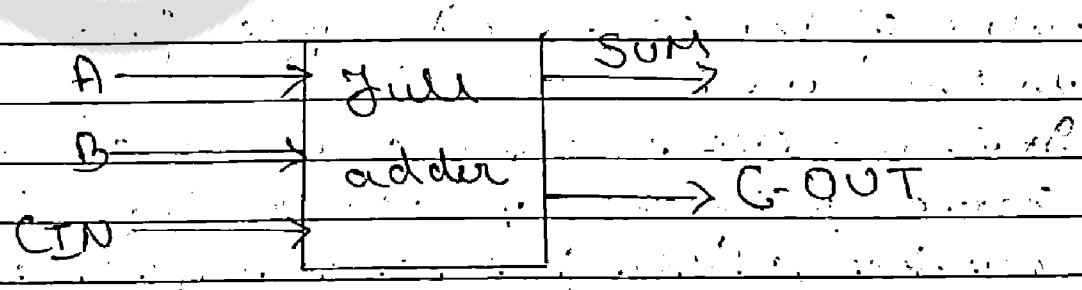
2 outputs S (SUM) and C (Carry). If A and B are the input bits, then the sum bit (S) is the X-OR of A and B and the carry bit (C) ~~is the~~ will be AND of A and B.

Truth Table

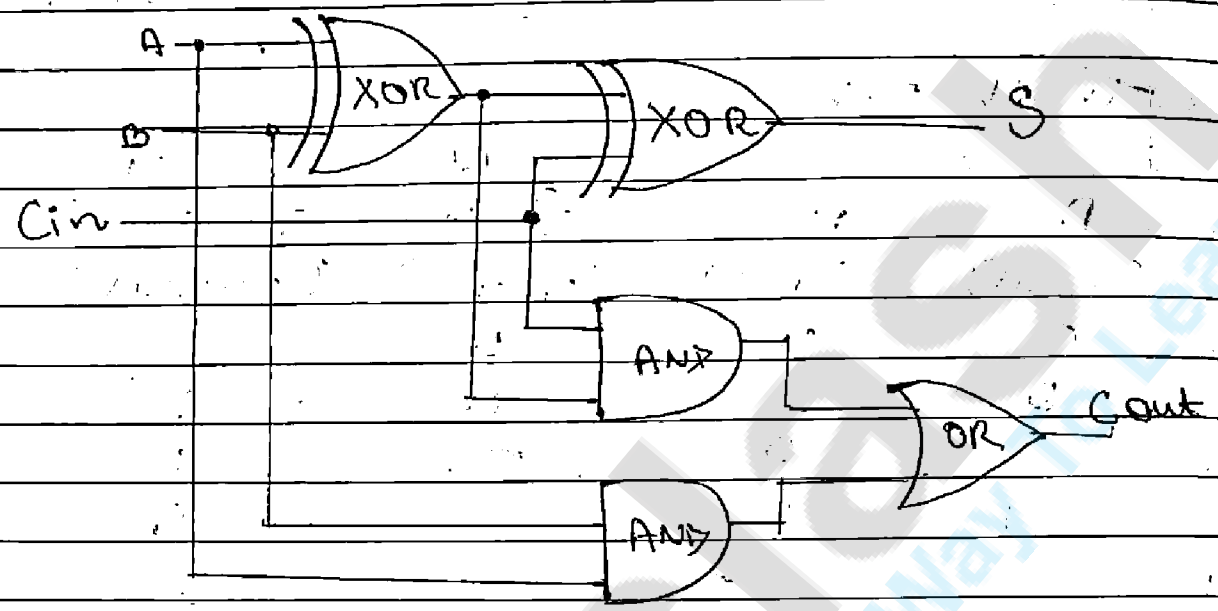
A (input)	B (input)	C — carry (output) → AND	S — sum (output) → XOR
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

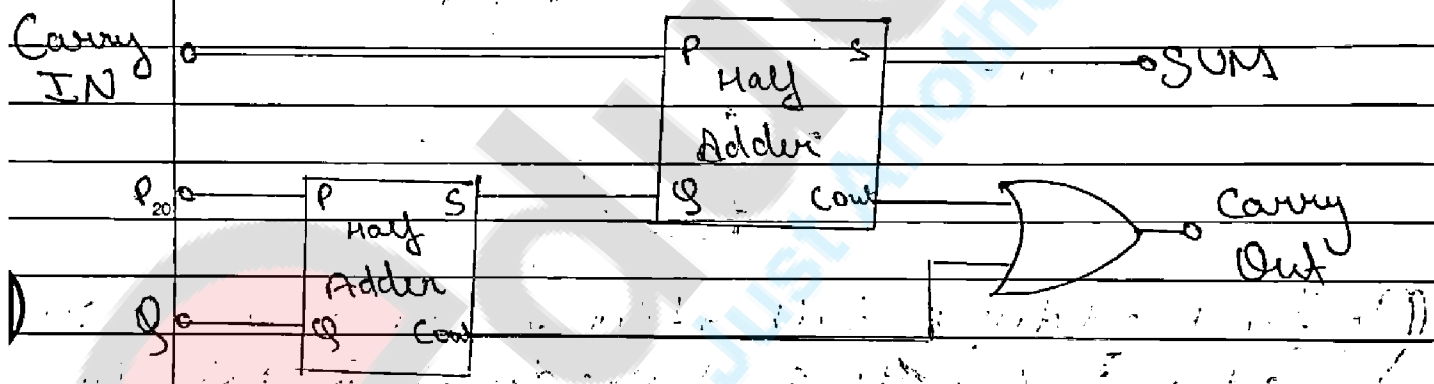


Q5) Full adder :- Full adder is the adder which adds 3 inputs and produces 2 outputs. The first 2 inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.



Full adders are commonly made from XOR, AND and OR gates in hardware.

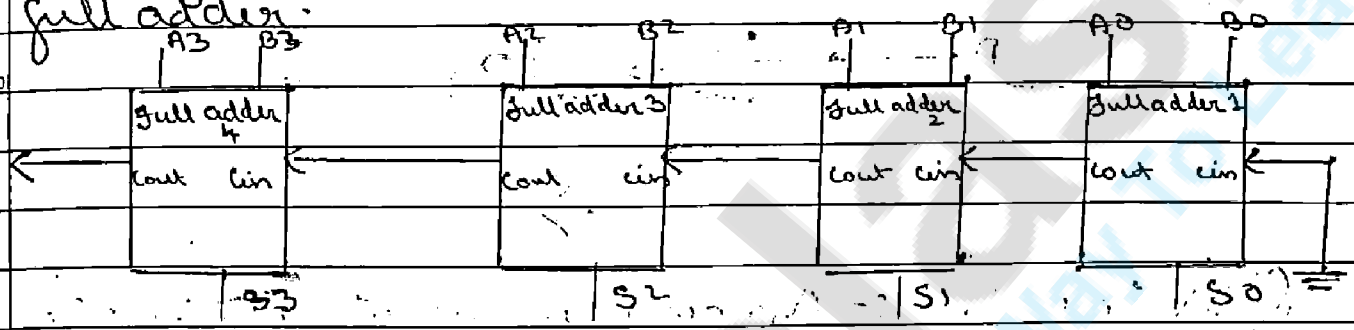




Q6] Ripple carry adder :- When multiple full adders are used with the carry ins and carry outs chained together then this is called a ripple carry adder because the correct value of the carry bit ripples from one bit to the next.

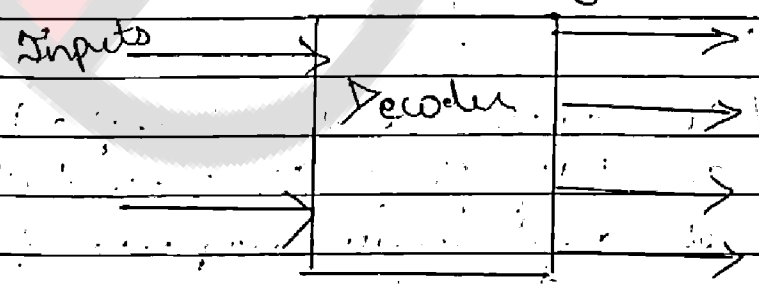
It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin

which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder. However, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.



4 bit ripple carry adder

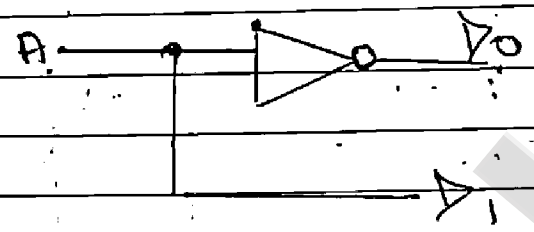
Q7) Decoder: The decoder is an electronic device that is used to convert digital signal to an analogue signal. It allows single input line and produce multiple output lines. The decoders are used in many communication project that are used to communicate between 2 devices. The decoder allows N-inputs and generates 2 power N-numbers of outputs. For eg:- If we give 2 inputs, that will produce 4 outputs by using 4 by 2 decoder.



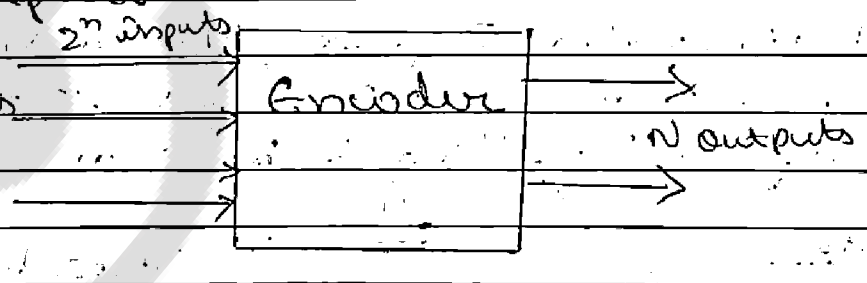
Truth Table

A	D_0	D_1
0	1	0
1	0	1

A is the address and D is the dataline. D_0 is NOT A and D_1 is A. The circuit looks like

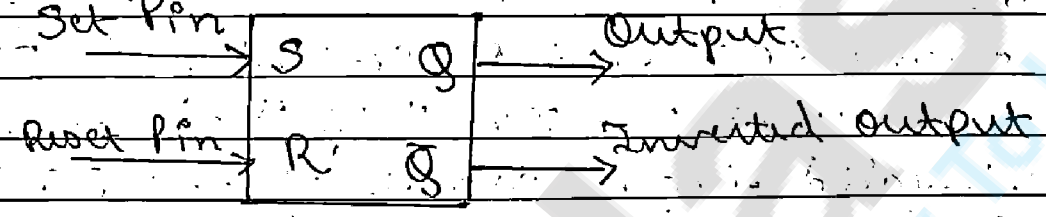


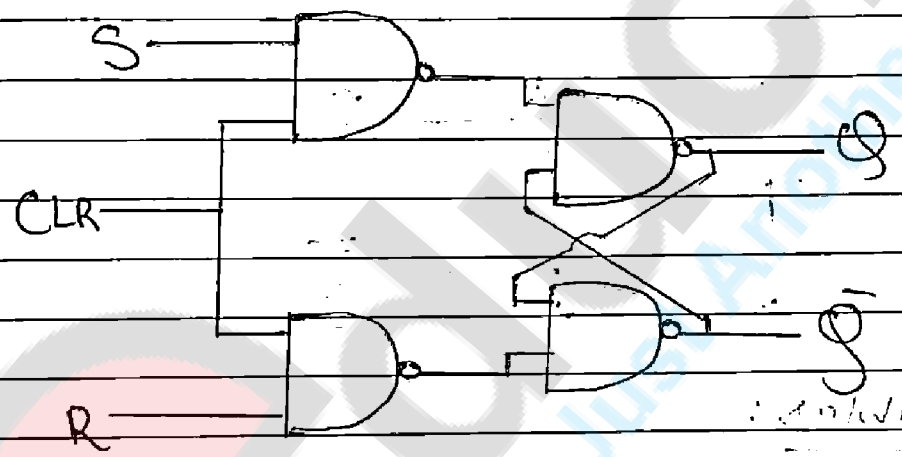
Q8) Encoder :- An encoder is an electronic device used to convert an analog signal to digital signal. It performs inverse operation of a decoder. It has a number of input lines but only one of the inputs is activated at a given time and produces an N-bit output code that depends on the activated input. For eg. in 4-2 encoder, if you gives n inputs, it produces only 2 outputs.



Q9) SR flip flop / SR latch :- Most simple type of flip flop is SR flip flop. It has two inputs S and R and two outputs Q and $\bar{Q}$. The state of this latch is determined by condition of Q. If Q is 1 the latch

is said to be SET and if Q is 0 the latch is said to be RESET. This SR latch or flip flop can be designed either by two cross-coupled NAND gates or two-cross coupled NOR gates. When we design this latch by using NAND gates, it will be active low S-R latch. That means it is SET when S=0. S-R Flip Flop is also called SET RESET flip-flop.

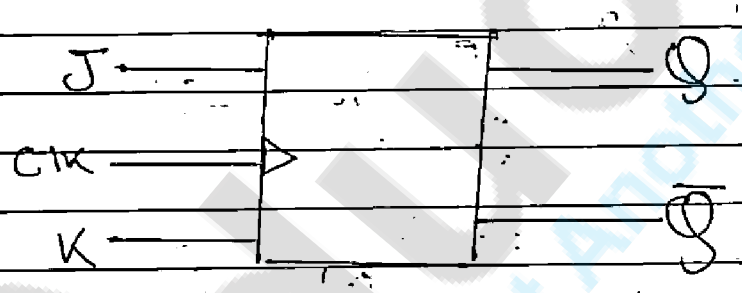




The 2 outputs shown above are inverse of each other

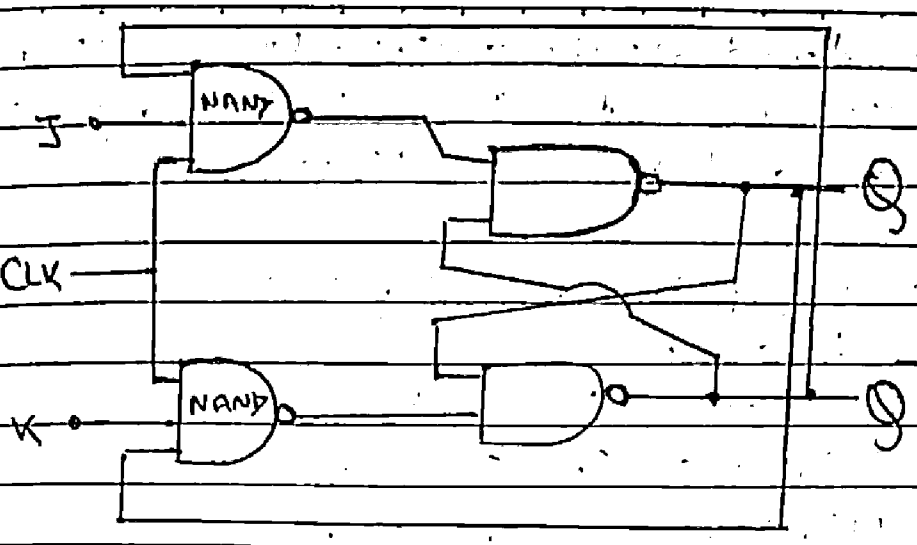
S	R	Q	$\bar{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

Q.10) **JK flip-flop** :- The JK flip-flop is also called as programmable flip-flop because, using its inputs, J, K, S and R, it can be made to mimic the action of any of the other flip flop types. The JK flip flop is the most widely used flip flop. It is considered to be a universal flip-flop circuit. The sequential operation of the JK flip flop is same as for the SR flip-flop with the same SET and RESET input. The difference is that the JK flip flop does not invalid input status of the SR latch (when S and R are both 1). The basic symbol of the JK flip flop is shown below.

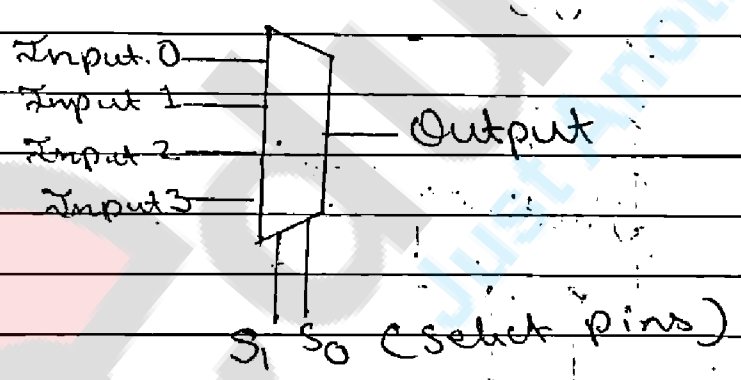


Truth Tables :-

J	K	CLK	Q	
0	0	↑	Q_0	(no change)
0	1	↑	0	
1	0	↑	1	
1	1	↑	$\overline{Q_0}$	(toggles)



(ii) Multiplexer:- Multiplexer is a device that has multiple inputs and a single line output. The select lines determine which input is connected to the output; and also to increase the amount of data that can be sent over a network within certain time. It is also called a data selector.



Multiplexer means many to one. Multiplexer handles 2 types of data that is analog and digital. The main purpose of multiplexer is to perform high speed switching. Multiplexers are capable of handling both analog and digital applications. In analog applications, multiplexers are made up of relays and transistor switches, whereas in digital applications, the multiplexers are built

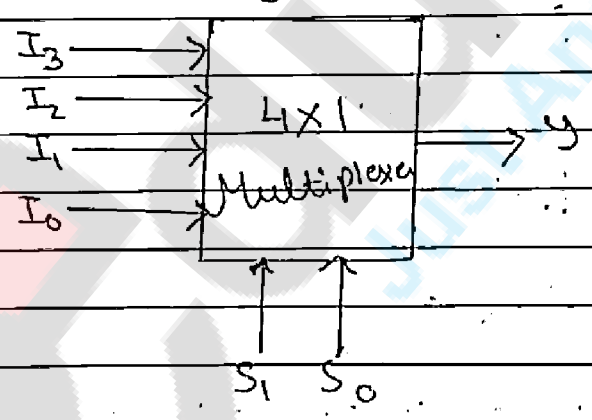
from standard logic gates. When the multiplexer is used for digital applications, it is called a digital multiplexer.

Multiplexer types :- Multiplexers are classified into four types :-

2-1 multiplexer (1 select line)
4-1 multiplexer (2 select lines)
8-1 multiplexer (3 select lines)
16-1 multiplexer (4 select lines)

4x1 Multiplexer :-

4x1 Multiplexer has four data inputs I_3, I_2, I_1 and I_0, two selection lines S_1 & S_0 and one output y. The block diagram of 4x1 multiplexer is shown in following figure :-



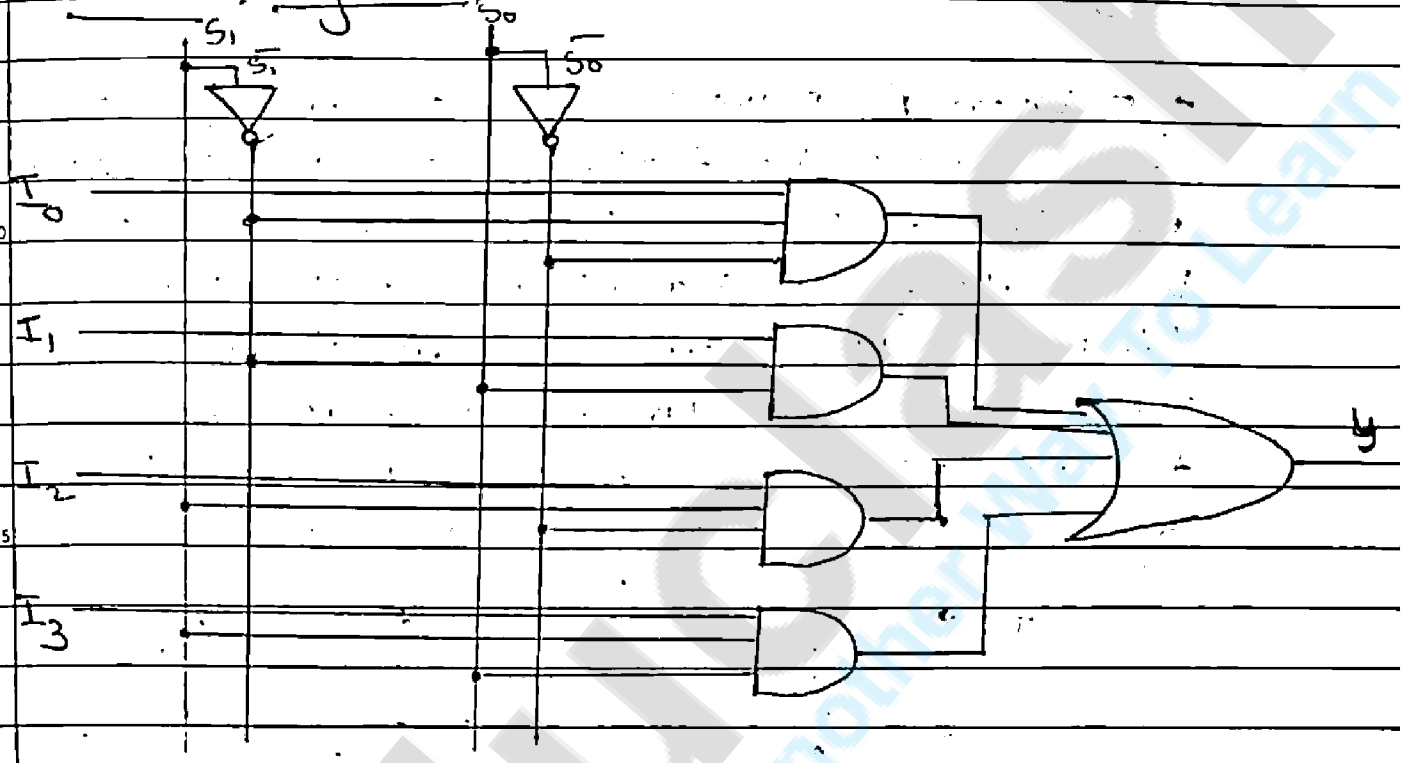
Truth table

Selection lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

From truth table, we can directly write the Boolean function for output y as

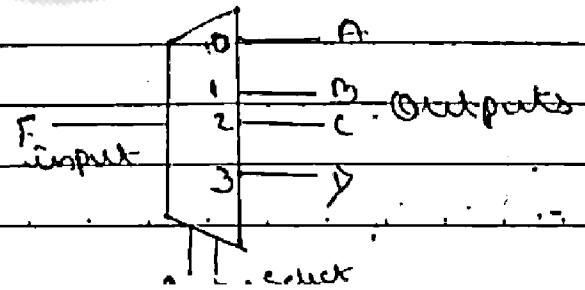
$$y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_2$$

Circuit Diagram



4×1 Multiplexer

(Q12) De-multiplexer :- De-multiplexer is also a device with one input and multiple output lines. It is used to send a signal to one of the many devices. The main difference between a multiplexer and a de-multiplexer is that a multiplexer takes 2 or more signals and encodes them on a wire, whereas a de-multiplexer does reverse to what the multiplexer does.



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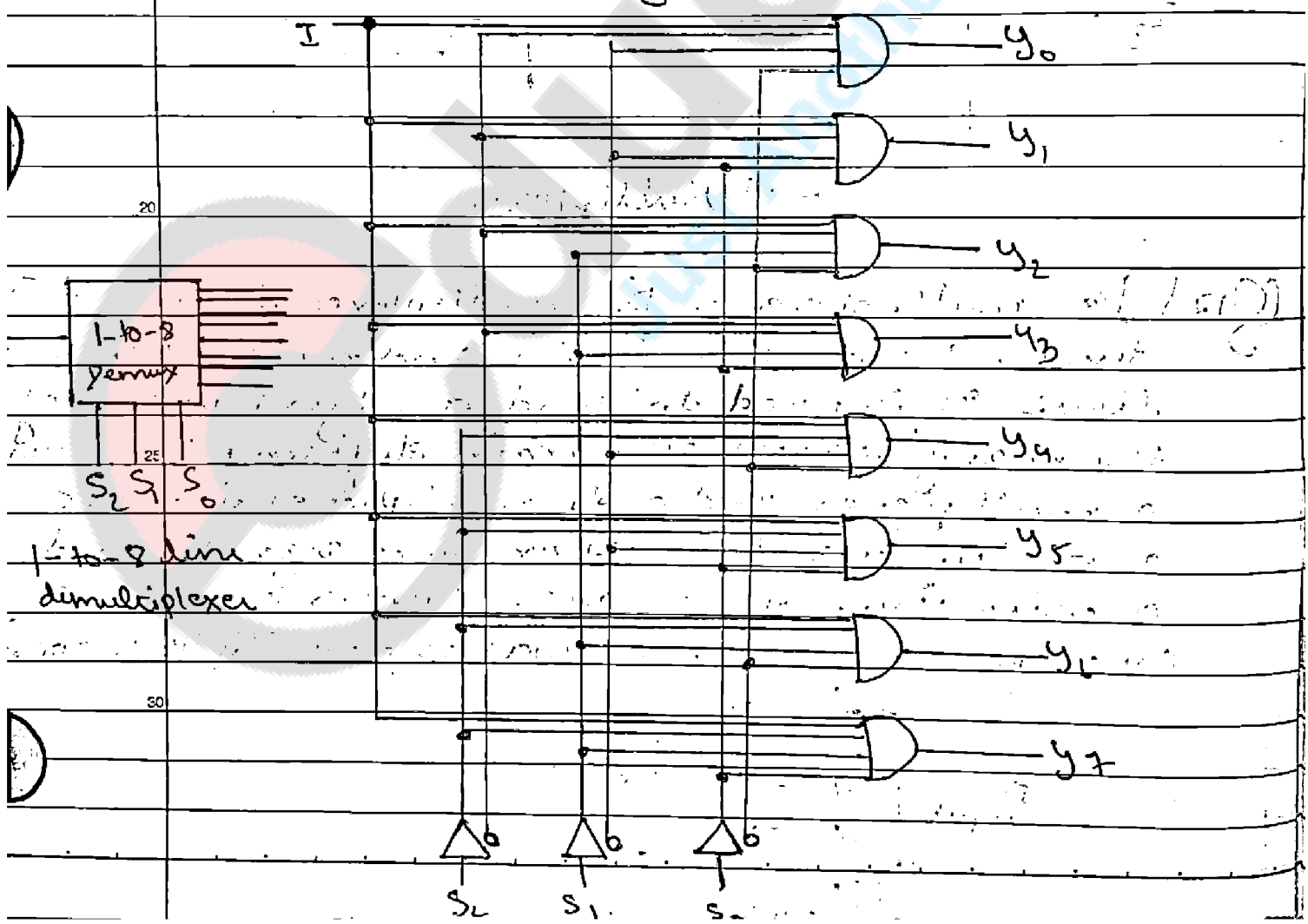
Types of De-multiplexer :- De-multiplexers are classified into four types

1) 1-2 demultiplexer (1 select line)
2) 1-4 demultiplexer (2 select lines)
3) 1-8 demultiplexer (3 select lines)
4) 1-16 demultiplexer (4 select lines)

1-8 De-multiplexers :- The demultiplexer is also called as data distributors as it requires one input, 3 selected lines and 8 outputs. De-multiplexer takes one single input data line and then switches it to any one of the output line. 1-to-8 demultiplexer circuit diagram is show below, it uses 8 AND gates for achieving the operation.



Truth Table

Data Input	Select Inputs			Outputs							
	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

$Y_0 = D\,\overline{S_2}\,\overline{S_1}\,\overline{S_0}$

$Y_1 = D\,\overline{S_2}\,\overline{S_1}\,S_0$

$Y_2 = D\,\overline{S_2}\,S_1\,\overline{S_0}$

$Y_3 = D\,\overline{S_2}\,S_1\,S_0$

$Y_4 = D\,S_2\,\overline{S_1}\,\overline{S_0}$

$Y_5 = D\,S_2\,\overline{S_1}\,S_0$

$Y_6 = D\,S_2\,S_1\,\overline{S_0}$

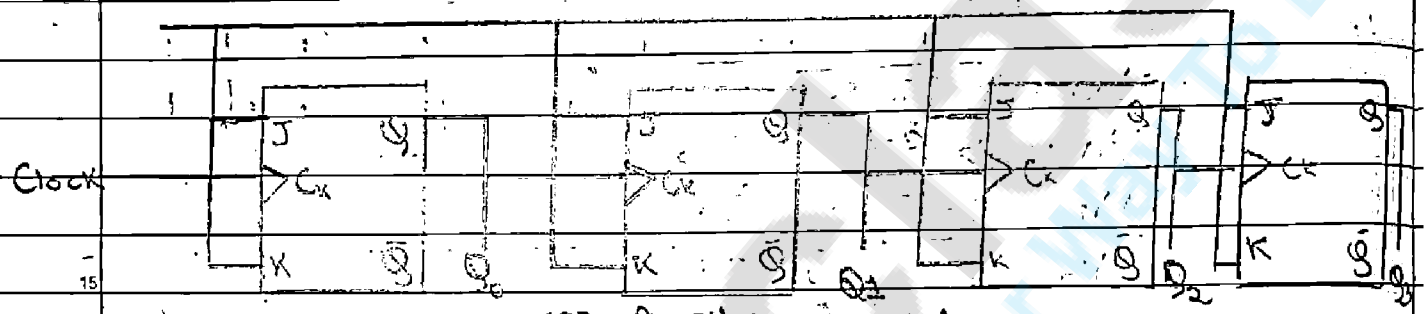
$Y_7 = D\,S_2\,S_1\,S_0$

Q13) Counters :- A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occured, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For eg., in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2... They can also be designed with the help of flip flops.

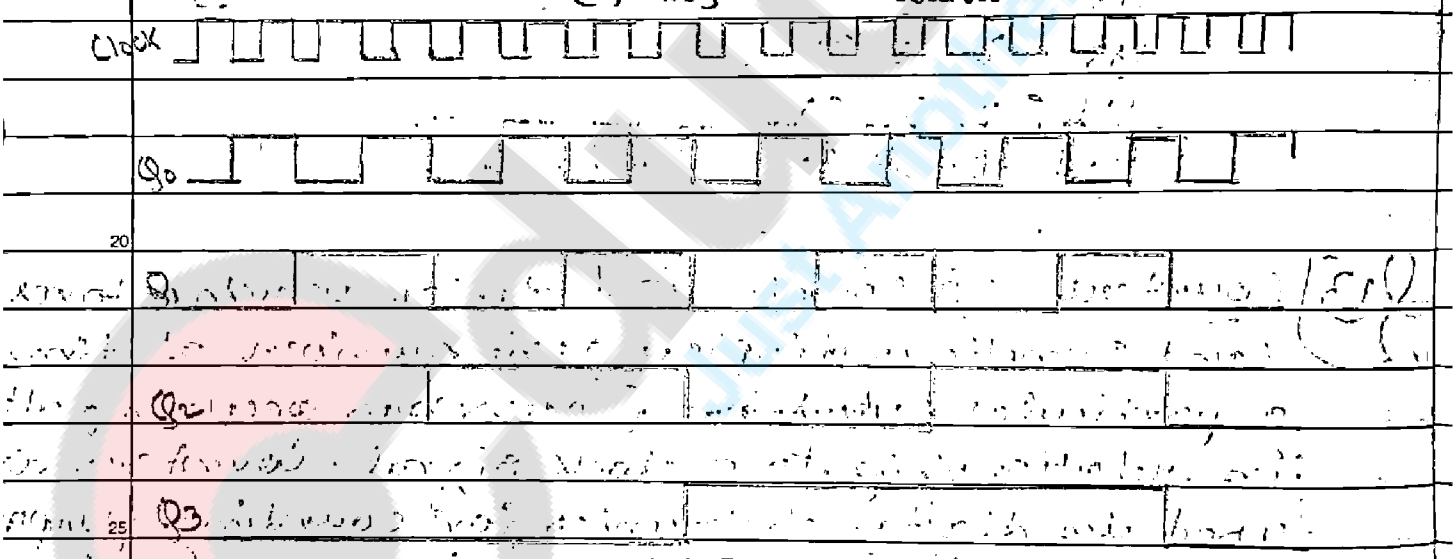
Counters are broadly divided into two catagories

1) Asynchronous counter
2) Synchronous counter

1) Asynchronous (Ripple) Counter :- In asynchronous counter we dont use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops. We can understand it by following diagram:-



(a) Asynchronous counter

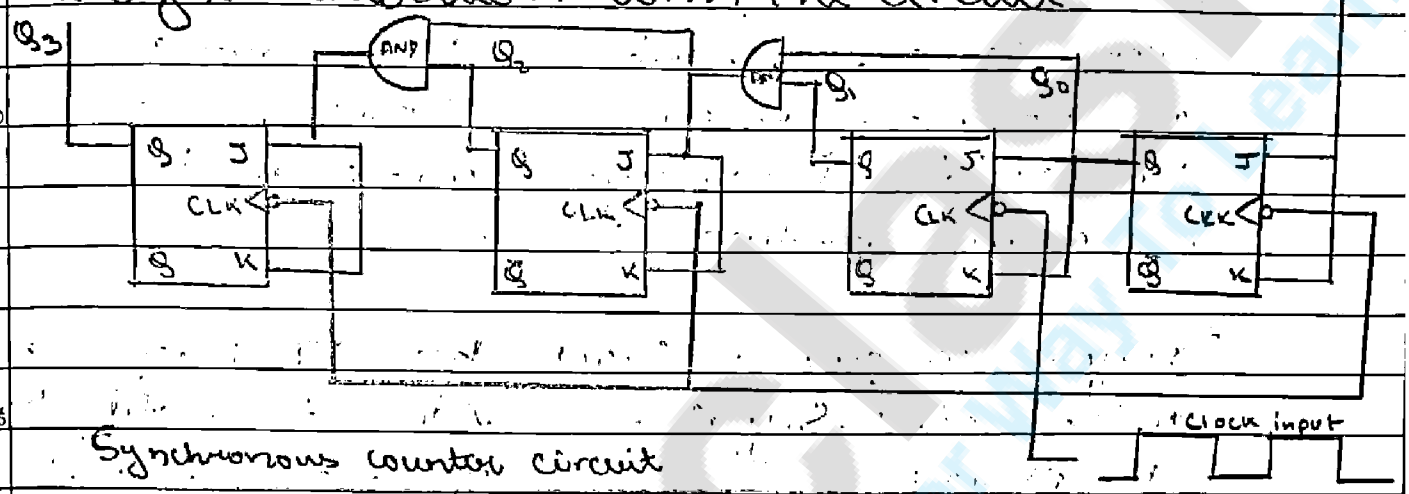


(b) Timing diagram

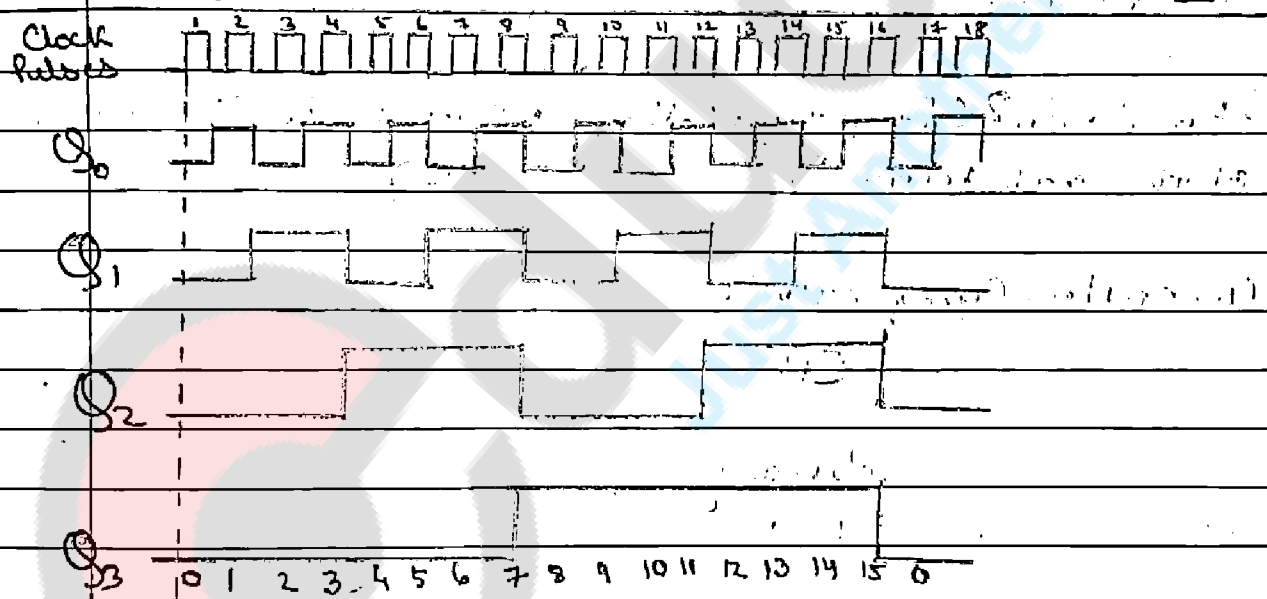
It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered (because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0, Q1, Q2, Q3 hence it is also

called RIPPLE counter.

② Synchronous Counter :- In synchronous counter all the flip flop's receive the external clock pulse simultaneously. Ring counter is the example of synchronous counters. In synchronous circuits, the external clock applied to all the flip flops is in synchronisation with the circuit.



Synchronous counter circuit



Timing diagram synchronous counter

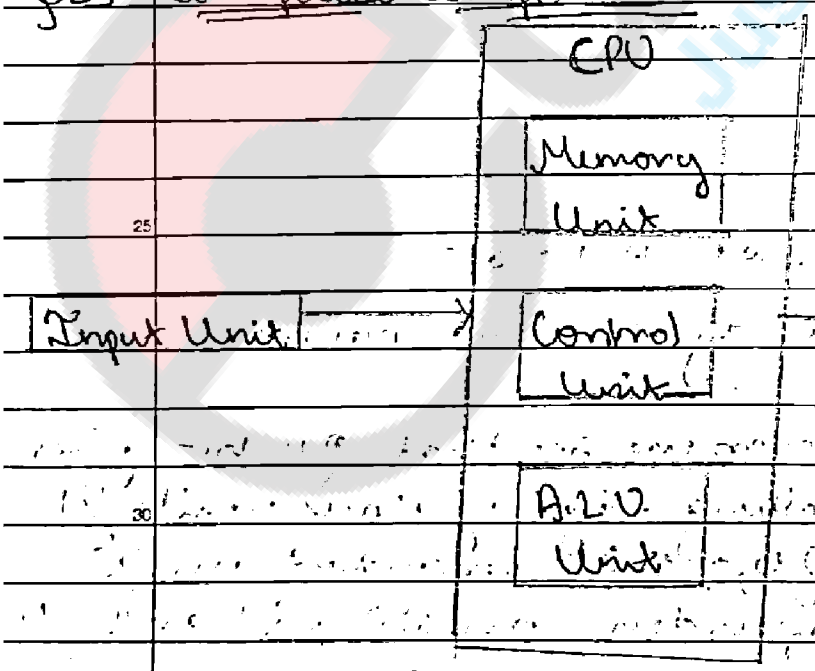
From circuit diagram we see that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0, Q3 is dependent on Q2, Q1 and Q0.

Unit 2

Q 1) Comparison of Computer Organization & Architecture

Computer Organization	Computer Architecture
1) Often called microarchitecture (low level)	Computer Architecture (a bit higher level)
2) Transparent from programmer (ex: a programmer does not worry much how addition is implemented in hardware)	Programmer view (i.e. Programmer has to be aware of which instruction set used)
3) Physical components (Circuit design, Address, Signals, Peripherals)	Logic (Instruction set, Addressing modes, Data types, Cache ~~Organ~~ Optimization)
4) How to do? (Implementation of the architecture)	What to do (Instruction set)

Q2) Computer Components



Input Unit :- This unit contains devices with the help of which we enter data into the computer. This unit creates a link between the user and the computer. The input devices translate the information into a form understandable by the computer.

CPU :- CPU is considered as the brain of the computer. CPU performs all types of data processing operations. It stores data, intermediate results and instructions (program). It controls the operation of all parts of the computer. CPU itself has 3 components :- 1) ALU 2) Memory Unit 3) Control Unit

1) ALU :- The Arithmetic logic Unit contains the electronic circuitry that executes all arithmetic & logical operations on the available data. It is used to perform all arithmetic calculations (+, −, ×, /) and logical calculation (<, >, =, AND, OR etc). logic unit performs comparison of numbers, letters and special characters. ALU uses registers to hold the data that is being processed.

2) Control Unit :- Control Unit co-ordinates with the input and output devices of a computer. It directs the computer to carry out stored program instructions by communicating with ALU & registers. It organizes the processing of data & instructions. To maintain the proper sequence of processing data, the control unit uses clock inputs.

3) Memory Unit :- Memory ~~unit~~ is the part of the computer which holds data and instructions. Memory is an integral component of the CPU. The memory unit consists of Primary memory & Secondary memory.

Primary Memory :- is used to store data and instructions during execution of the instru

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ctions Types < RAM < SRAM, DRAM
ROM < PROM, EPROM, EEPROM

Secondary Memory:- Used to store data and instructions permanently. eg:- Hard Disk, CD, DVD etc.

3) Output Unit :- The output unit consists of devices with the help of which we get the information from the computer. This unit is a link between the computer and the users. The output devices translates the computers output into a form understandable by the users.

Q3) Computer functions/Basic instruction cycle

Basic functions that computer performs in general are :-

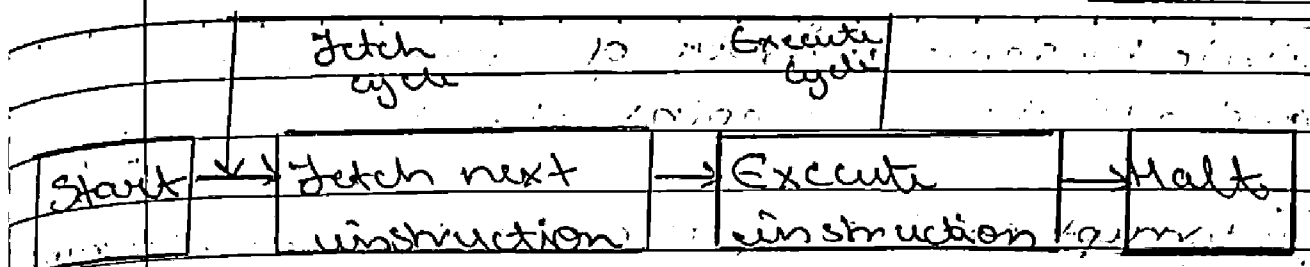
1) Data processing :- is the process of gathering and storing data

2) Data storing :- used for storing and managing the data which are processed by data processing functions.

3) Data movement :- Computer is able to move the data from one device to another device. The movement of data from one peripheral device to another device are also called as data communication.

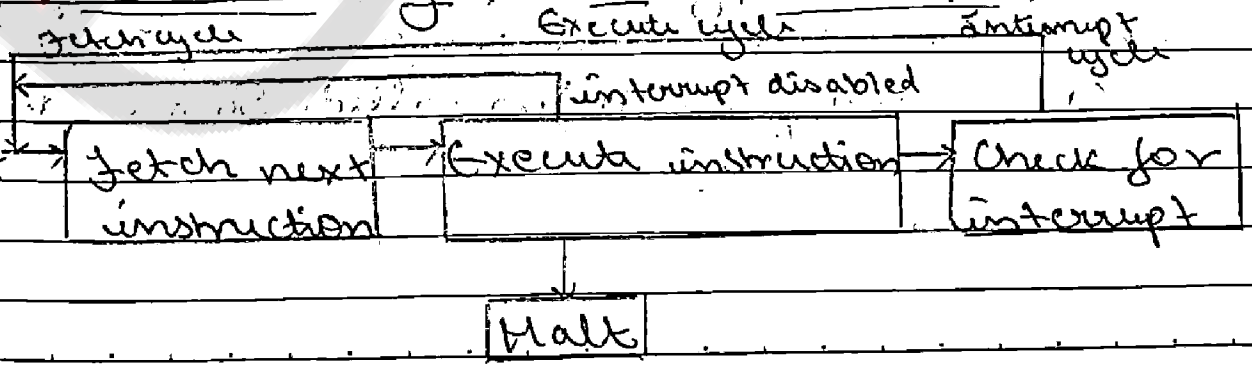
4) Control :- For controlling over all the process control functions are used.

Instruction cycle :-



Instruction cycle is referred to as Fetch cycle & Execute cycle.
At the beginning of each instruction cycle the processor fetches instruction from memory. The program counter holds the address of the instruction to be fetched, processor always increments the program counter so that it will fetch the next instruction in sequence.
(a) In execution of instruction 4 categories are there:- 1) Processor memory:- Data transfer happening from processor to memory or from memory to processor.
2) Processor I/O:- In this data can be transferred between two devices.
3) Data processing:- Processor may perform some arithmetic or logical operation.
4) Control:- Instruction specifying the sequence of execution.
Program instruction halts only if the system turn off or some error may come.

Q4) Instruction cycle with interrupt :-



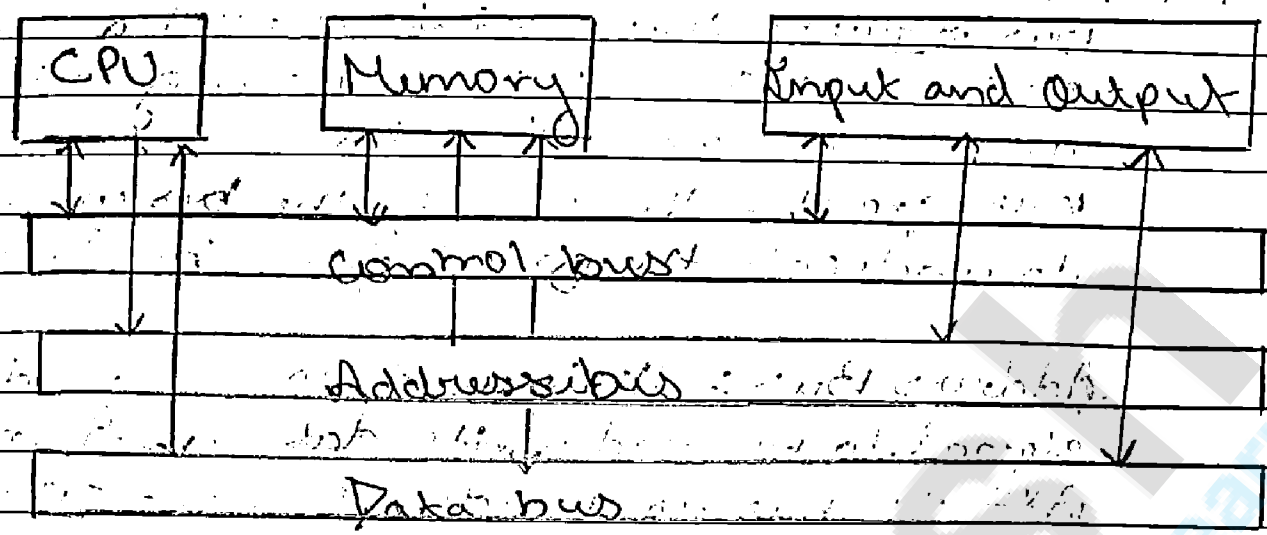
Write the same answer of instruction cycle and add the below point of interrupt cycle

Interrupt cycle :- Processor checks for interrupt indicated by interrupt signal. If no interrupt, fetch next instruction. And if interrupts is pending suspend the execution of program and interrupt handler comes in place.

Q5) Interconnection Structures / System Bus / Bus Interconnection / Bus Structure

Interconnection Structures :- A computer consists of a set of components (CPU, memory, I/O) that communicate with each other. The collection of paths connecting the various modules is called the interconnection structure. The design of this structure will depend on the exchange that must be made between modules. Type of transfers :- Memory to CPU, CPU to Memory, I/O to CPU, CPU to I/O, I/O to or from Memory (DMA)

Bus Interconnection :- A bus is a communication pathway connecting two or more devices. It is a shared transmission medium. A bus consists of multiple pathways or lines. A bus that connects major components (CPU, Memory, I/O) is called System Bus.



System Bus

Combination of control bus, Address bus and data bus is called system bus.
It is divided into 3 main categories
1) Control Bus 2) Address Bus, 3) Data Bus

Control Bus :- These lines are used to transfer control signal from one component to another. It specifies the type of operation that is to be performed. When CPU gives command to the memory for writing data, then memory sends acknowledgement signal to CPU after successful writing of data. Also controls use of data and address lines. Typical control lines include
Memory write :- It is used to write data to a given memory location.
Memory read :- It is used to read from a given memory location.
I/O write :- It is used to write some data on output device.
I/O Read :- It is used to read some data on output device.

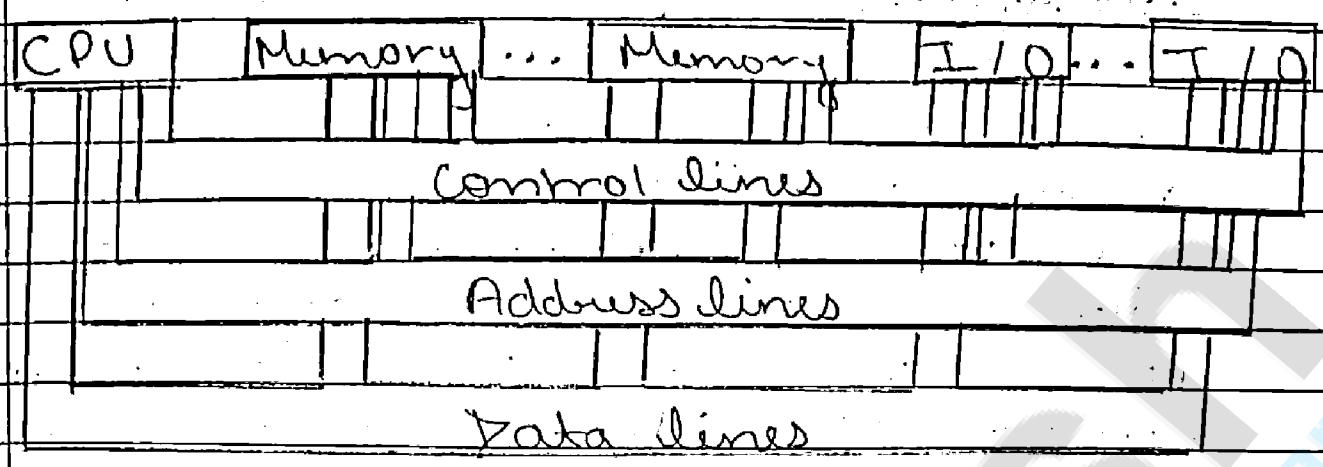
Bus request:- It is used to request a control on the bus so that the requesting device can use it to transmit data.

Bus grant:- It is used by the bus controller to indicate the grant of the bus to a device.

Address Bus:- It is used to carry address signal to ~~wr~~ read write data in the memory. Address bus is unidirectional. When a component of a computer want to communicate with another, it uses a few system bus lines to specify an address of destination. These lines are called address bus. It identifies the source or destination of data carried by data bus.

Data Bus:- Data bus is used to transfer the data from one component to another. There are 32 or 64 parallel lines of data bus. The amount of data that a bus can transmit is called bus-width. A 64 line data bus can ~~transfer~~ transmit 64 bits (8 bytes) at a time. Width of data bus has direct impact on the performance of the computer. Data bus is bi-directional.

Bus interconnection Structure | Scheme:-
A bus is a communication pathway connecting 2 or more devices. A bus consists of multiple pathways or lines. A bus that connects major components (CPU, Memory, I/O) is called Bus Structure.



~~22 Fra~~ Each line is assigned a particular meaning of function. These lines can be classified into 3 functional groups 1) Data line 2) Address line 3) Control line

[Write the answer of Data bus, Address bus and Control bus for Data line, Address line, Control line respectively.]

Q6) Functions of I/O module :- I/O modules are the critical element of the computer system after CPU and memory. All computer systems must have effective means to receive input and deliver output. Wide variety of peripherals in different amounts of data, at different speeds and in different formats, all are slower than CPU and RAM. Input-output module provides a method for transferring information between internal storage and external I/O devices. Some of the important functions of an Input-Output (I/O) module are as follows :-

1) Control and timing
2) Processor communication
3) Device communication
4) Data buffering
5) Error detection

1) Control & timing :- The I/O module must be able to co-ordinate the flow of data between the internal resources (such as processor, memory) and external devices.

2) Processor communication :- This involves the following tasks : (a) Exchange of data between processor and I/O module. (b) command decoding :- I/O module accepts commands sent from the processor. Eg, the I/O module for a disk drive may accept the following commands from the processor : READ SECTOR, WRITE SECTOR, SEEK track etc. (c) status reporting :- The device must be able to report its status to the processor, eg, disk drive busy, ready etc. Status reporting may also involve reporting various errors. (d) Address recognition :- Each I/O device has a unique address and the I/O module must recognize this address.

3) Device communication :- The I/O module must be able to perform device communication such as status reporting.

4) Data buffering :- This is necessary as there is a speed mismatch between speed of data transfer between processor and memory and external devices. Data coming from the main memory are sent to an I/O module in a rapid burst. The data is buffered in the I/O module and then sent to the peripheral device at its rate.

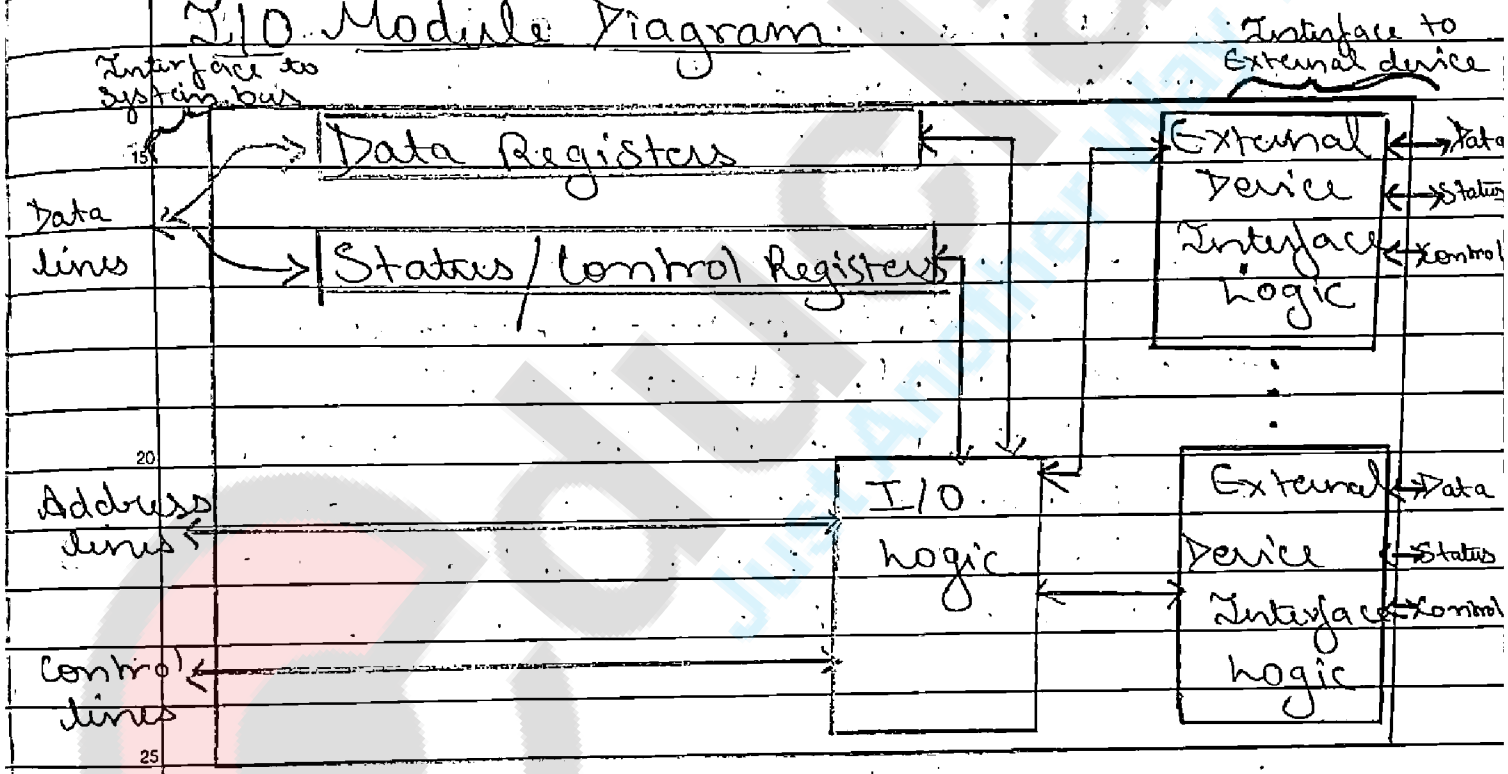
5) Error detection :- The I/O module must also be able to detect errors and report them to the processor. These errors may

be mechanical errors (such as paper jam in a printer), or changes in the bit pattern of transmitted data. A common way of detecting such errors is by using parity bits.

I/O Steps:-

1) CPU checks I/O module device status
2) I/O module returns status
3) If ready, CPU requests data transfer
4) I/O module gets data from device
5) I/O module transfers data to CPU.

I/O Module Diagram



Input Output Techniques

1) Programmed I/O
2) Interrupt driven I/O
3) Direct Memory Access (DMA)

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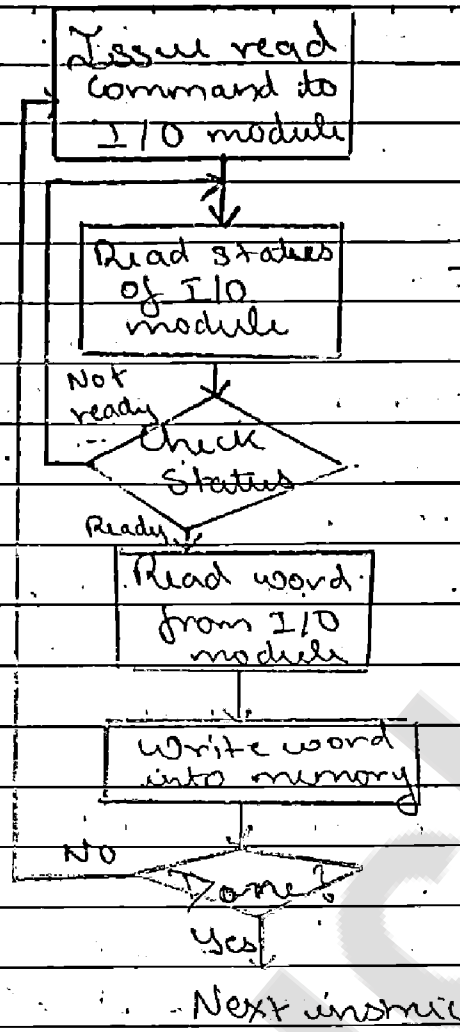
(F) Programmed I/O:- Programmed I/O refers to data transfers initiated by a CPU to access registers or memory on a device.
The CPU issues a command then waits for I/O operations to be complete. As the CPU is faster than the I/O module, the problem with programmed I/O is that the CPU has to wait a long time for the I/O module of concern to be ready for either reception or transmission of data. The CPU, while waiting, must repeatedly check the status of the I/O module and this process is known as Polling. As a result, the level of the performance of the entire system is severely degraded.
Programmed I/O basically works in these ways:-

1) CPU requests I/O operation
2) I/O module performs operation
3) I/O module sets status bits
4) CPU checks status bits periodically
5) I/O module does not inform CPU directly
6) I/O module does not interrupt CPU
7) CPU may wait or come back later.

Programmed I/O Mode Input Data Transfer :-



Q8] Interrupt driven I/O :- The problem with programmed I/O is that the processor has to wait a long time for the I/O module of concern to be ready for either reception or transmission of data. The solution to this problem is to provide an interrupt mechanism. In this approach the processor issues an I/O command to a module and then go on to do some other useful work. The I/O module ~~with~~ will then interrupt the processor to request service when it is ready to exchange data with the processor. The processor then executes resumes its former processing.

Let us consider how it works

a] From the point of view of the I/O module:-

For input, the I/O module services a READ command from the processor.
The I/O module then proceeds to read data from an associated peripheral device.
Once the data are in the modules data register, the module issues an interrupt to the processor over a control line.
The module then waits until its data are requested by the processor.
When the request is made, the module places its data on the data bus and is then ready for another I/O operation.

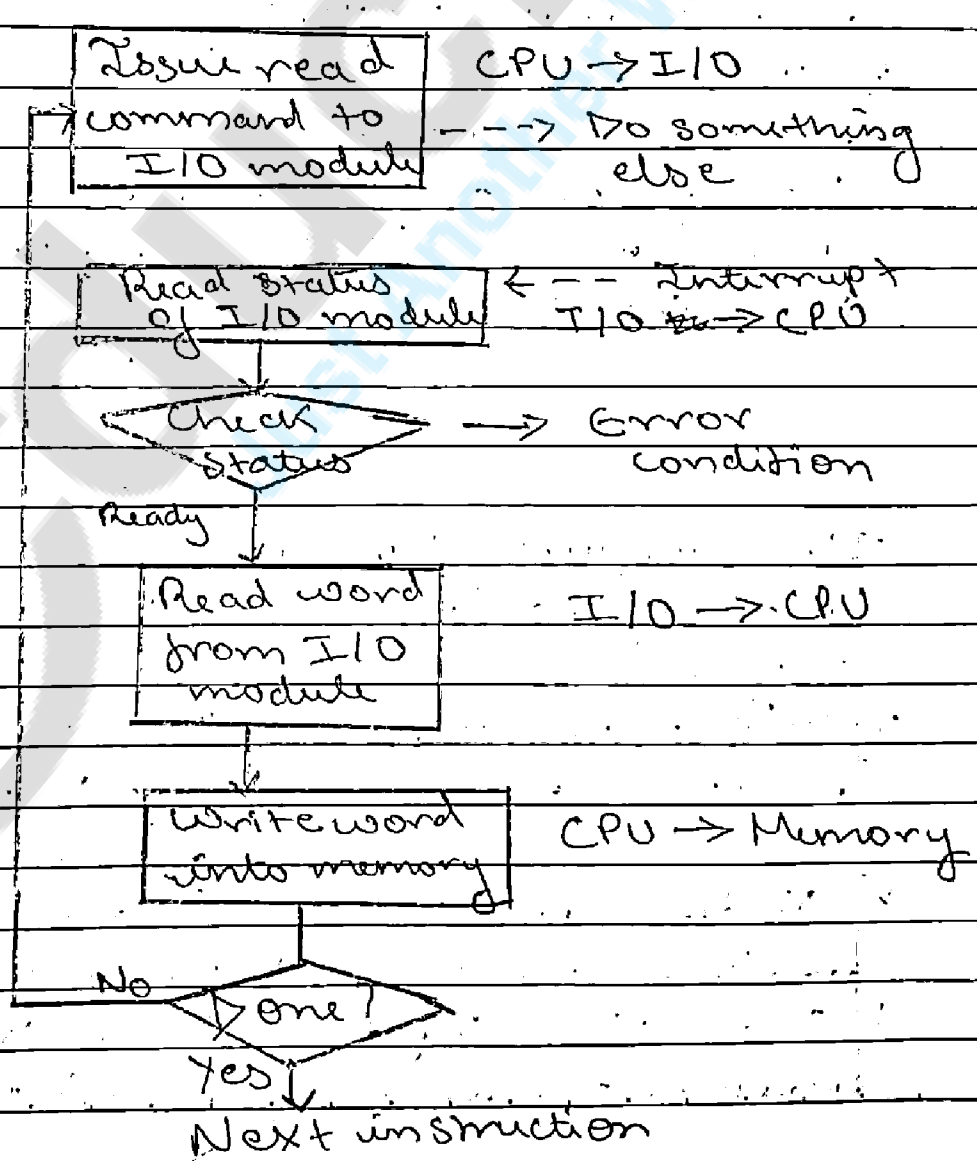
b) From the processor point of view, the action for an input is as follows:
The processor issues a READ command.
It then does something else (eg. the processor may be working on several different programs at the same time)
At the end of each instruction cycle, the processor checks for interrupts.
When the interrupt from an I/O module occurs, the processor saves the context (eg program counter & processor registers) of the current program and processes the interrupt.
In this case, the processor reads the word of data from the I/O module and stores it in memory.
It then restores the context of the program it was working on and resumes execution.

Below are the basic operations of Interrupt:

1) CPU issues read command
2) I/O module gets data from peripheral whilst CPU does other work
3) I/O module interrupts CPU
4) CPU requests data
5) I/O module transfers data

Design issues for Interrupt:-

There are 2 main problems for interrupt I/O :-
1) There are multiple I/O modules; how does the processor determine which device issued the interrupt?
2) If multiple interrupts have occured how the processor does decide which one to process?

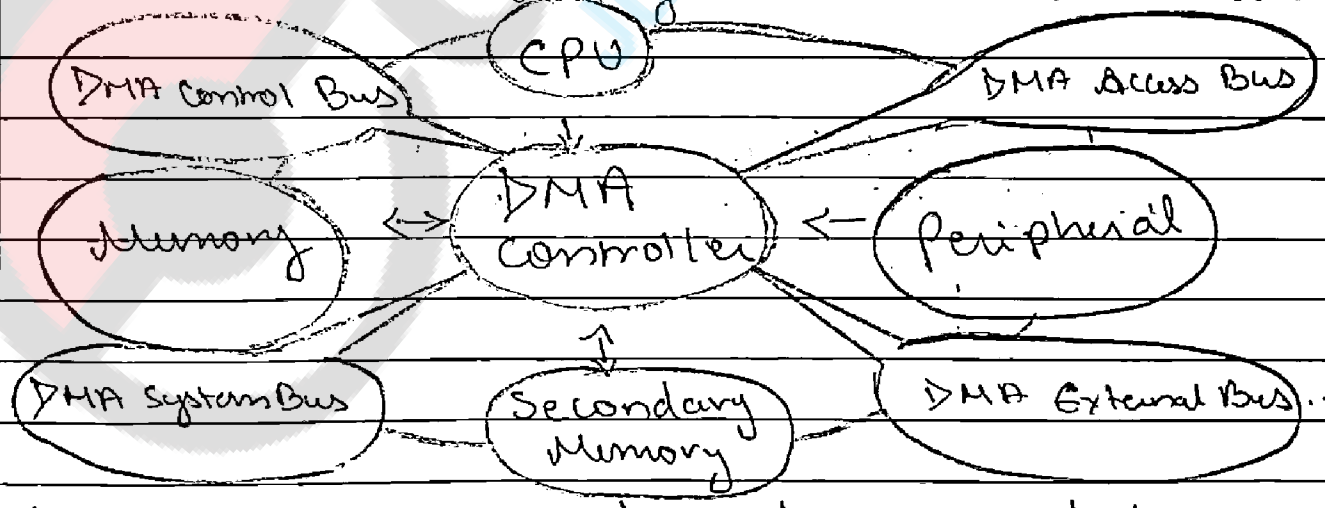


Q9) Compare Programmed I/O with Interrupt Driven I/O

	Programmed I/O	Interrupt Driven I/O
1)	In programmed IO, processor has to check each I/O device in sequence and in effect 'ask' each one if it needs communication with the processor. The checking is achieved by continuous polling cycle and hence processor can not execute other instruction in sequence.	External asynchronous input is used to tell the processor than I/O device needs its service and hence processor does not have to check whether I/O device needs its service or not.
2)	During polling processor is busy and therefore, have serious and detrimental effect on system throughput.	In interrupt driven I/O, the processor is allowed to execute its instructions in sequence and only stop to service I/O device when it is told to do so by the device itself. This increases system throughput.
3)	It is implemented without interrupt hardware support	It is implemented using interrupt hardware support
4)	It does not depend on interrupt status	Interrupt must be enabled to process interrupt driven I/O
5)	It does not need ~~an~~ initialization of stack	It needs initialization of stack.
6)	System throughput decreases as number of	System throughput does not depend on number of I/O

I/O devices connected in the system increases	devices connected in the system

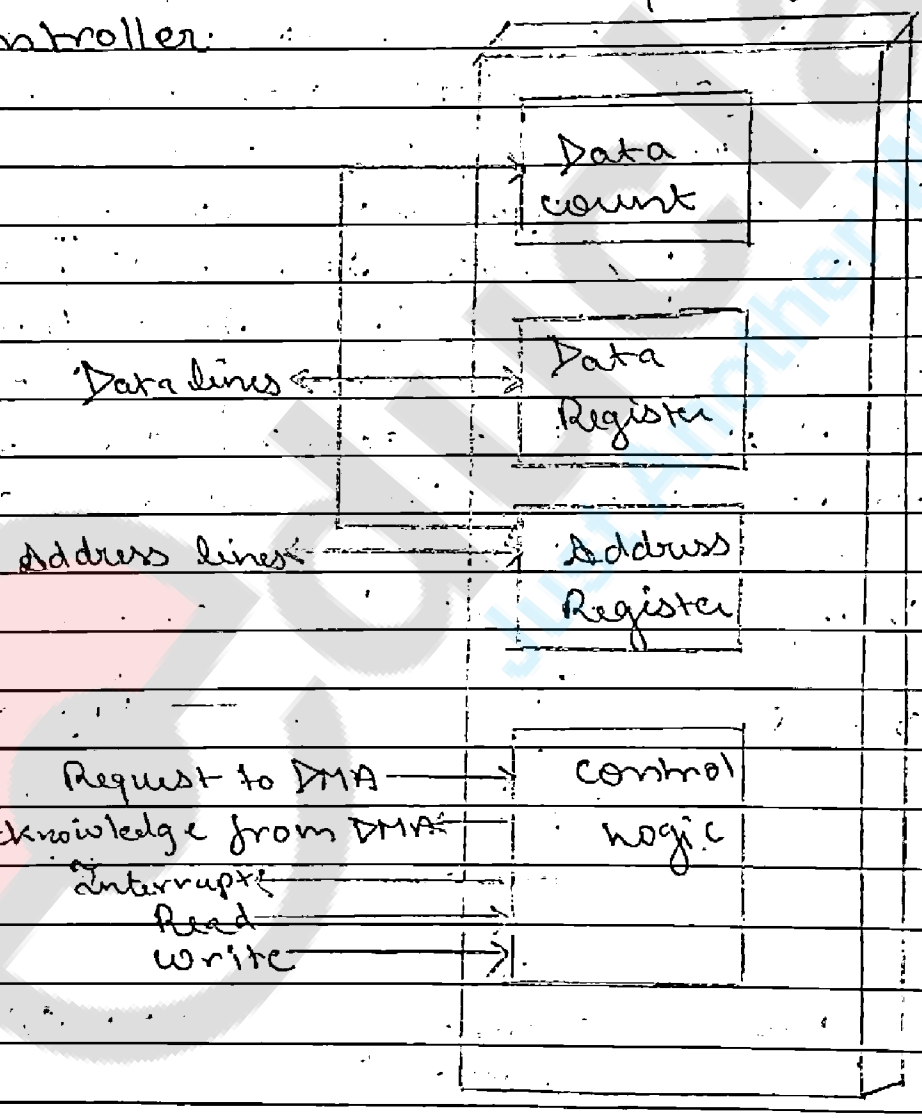
Q10) Direct Memory Access (DMA) :- DMA stands for "Direct Memory Access" and is a method of transferring data from the computer's RAM to another part of the computer without processing it using the CPU. While most data that is input or output from your computer is processed by the CPU, some data does not require processing or can be processed by another device.
In these situations, DMA can save processing time and is a more efficient way to move data from the computer's memory to other devices. In order for devices to use direct memory access, they must be assigned to a DMA channel. Each type of port on a computer has a set of DMA channels that can be assigned to each connected device. For example, a PCI controller and a hard drive controller each have their own set of DMA channels.



For example, a sound card may need to access data stored in the computer's RAM, but since it can process the data itself, it may use

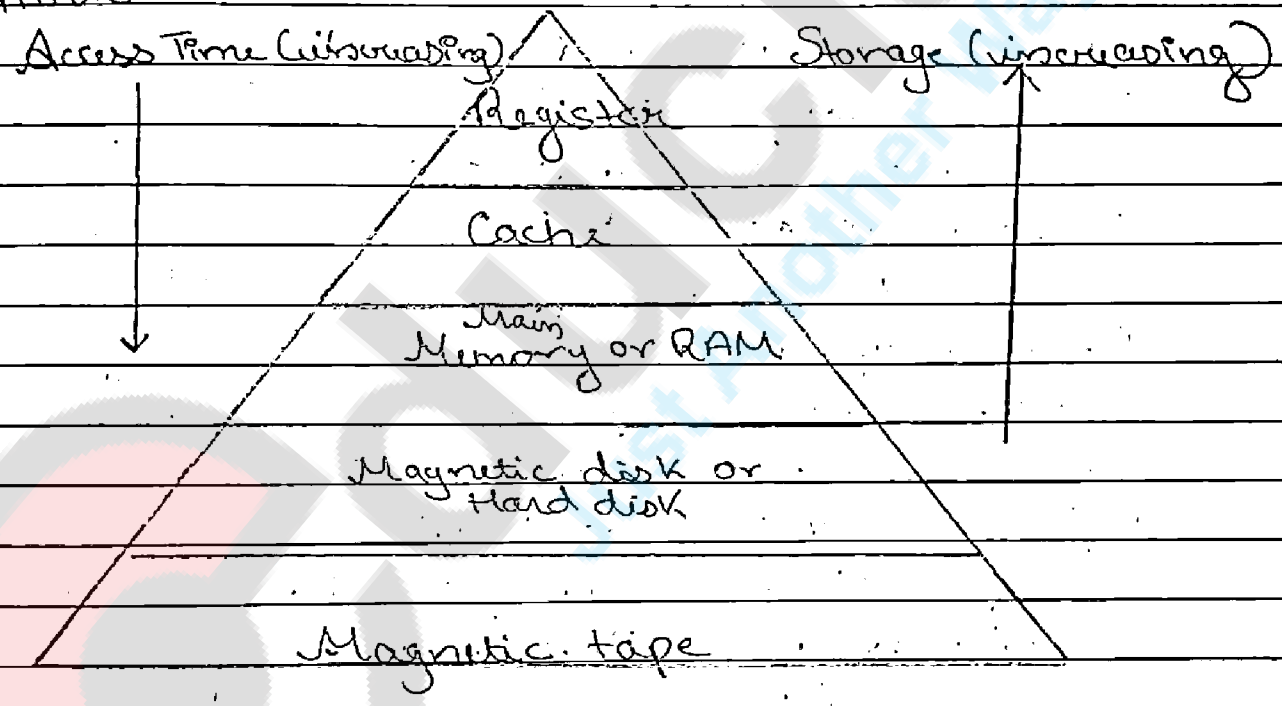
DMA to bypass the CPU. Video cards that support DMA can also access the system memory and process graphics without needing the CPU.

With DMA, the CPU can process other tasks while data transfer is being performed. The transfer of data is first initiated by the CPU. During the transfer of data between the DMA channel and I/O device, the CPU performs other tasks. When the data transfer is complete, the CPU receives an interrupt request from the DMA controller.



Unit 3

Q1] Memory Hierarchy :- The memory unit is used for storing programs and data. It fulfills the need of storage of the information.
The additional storage with main memory capacity enhance the performance of the general purpose computers and make them efficient.
Only those programs and data, which is currently needed by the processor, reside in main memory.
Information can be transferred from auxiliary memory to main memory when needed.
The memory system is a hierarchy of storage devices with different capacities, costs and access times.



1) Registers :- CPU registers are at the top most level of this hierarchy, they hold the most frequently used data. They are very limited in number and are the fastest.
They are often used by the CPU and the ALU for performing arithmetic and logical operations for temporary storage of data.

2) Cache :- is used by the CPU for memory which is being accessed over and over again. Instead of pulling it every time from the main memory, it is put in cache for fast access. It is also a smaller memory, however larger than internal registers.

Cache is further classified to L1, L2 and L3:

a) L1 cache :- It is accessed without any delay.

b) L2 cache :- It takes more clock cycles to access than L1 cache

c) L3 cache :- It takes more clock cycles to access than L2 cache.

3) Main Memory :- or RAM (Random Access Memory) :- The memory unit that communicates directly within the CPU, Auxiliary memory and Cache memory is called main memory. It is the central storage unit of the computer system. It is a large and fast memory used to store data during computer operations. It is a type of the computer memory and is a hardware component. It can be increased provided the operating system can handle it.

4) Hard disk :- A hard disk is a hardware component in a computer. Data is kept permanently in this memory. Memory from hard disk is not directly accessed by the CPU, hence it is slower. As compared with RAM, hard disk is cheaper per bit.

5) Magnetic tape :- Magnetic tape memory is usually used for backing up large data. When the system needs to access a tape, it is first mounted to access the data. When the data is accessed, it is unmo-

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unit d. The memory access time is slower in magnetic tape and it usually takes few minutes to access a tape.

Q2). RAM and its types :- It is also called "direct access memory." Random access means that each individual byte in entire memory can be accessed directly. RAM is used to store data and instructions temporarily. A program must be loaded into RAM before execution.

RAM is volatile memory. It means that it contents are lost when the power is turned off. RAM is read/write memory. CPU can read data from RAM and write data to RAM. It is used to store data and instruction while it is being executed. RAM is also called main memory or primary storage. RAM plays very important role in the processing speed of a computer. A bigger RAM size provides larger amount of space for processing. So the processing speed is increased. The amount of data that can be stored in RAM is measured in bytes. Most desktop computers typically have 2 to 4 GB of RAM. It also allows the addition of more memory if needed.

Types of RAM :-

1) DRAM (Dynamic Random Access Memory) :-
DRAM stands for Dynamic Random Access Memory. It is used in most of the computers. It is the least expensive kind of RAM. It requires an electric current to maintain its electrical state. The electrical charge of DRAM decreases with time that may

result in loss of DATA. DRAM is recharged or refreshed again and again to maintain its data. The processor cannot access the data of DRAM when it is being refreshed. That is why it is slow.

2) SRAM :- SRAM stands for Static Random Access Memory. It can store data without any need of frequent recharging. CPU does not need to wait to access data from SRAM during processing. That is why it is faster than DRAM. It utilizes less power than DRAM. SRAM is more expensive as compared to DRAM. It is normally used to build a very fast memory known as cache memory.

3) MRAM (Magneto resistive Random Access Memory) :- MRAM stands for Magneto resistive Random Access Memory. It stores data using magnetic charges instead of electrical charges. MRAM uses far less power than other RAM technologies so it is ideal for portable devices. It also has greater storage capacity. It has faster access time than RAM. It retains its contents when the power is removed from computer.

Q3) Difference between SRAM and DRAM

SRAM :- It is faster than DRAM
It is more expensive as compared to DRAM.
It does not need to be power-refreshed.
It utilizes less power.
It holds data indefinitely as long as the computer is turned on.

It is more complex and less compact.
Used in cache memory
DRAM:-
It is slower than SRAM
It is less expensive
It has to be refreshed after each read operation.
It utilizes more power.
It holds data dynamically not indefinitely.
It is less complex and more compact.
Used in main memory.

Q4) ROM and its types:- ROM stands for Read Only Memory. The memory from which we can read but cannot write on it. This type of memory is non-volatile. The information is stored permanently in such instructions that are required to start a computer. This operation is referred to as bootstrap.
ROM is further classified into 3 types -
PROM:- Short for programmable read-only memory, a memory chip on which data can be written only once. Once a program has been written onto a PROM, it remains there forever. Unlike RAM, PROMs retain their contents when the computer is turned off. The difference between a PROM and a ROM is that a PROM is manufactured as blank memory, whereas a ROM is programmed during the manufacturing process. To write data onto a PROM chip, you need a special device called a PROM programmer or PROM burner.
EPROM:- Acronym for Erasable Programmable Read Only Memory: EPROM is a special type

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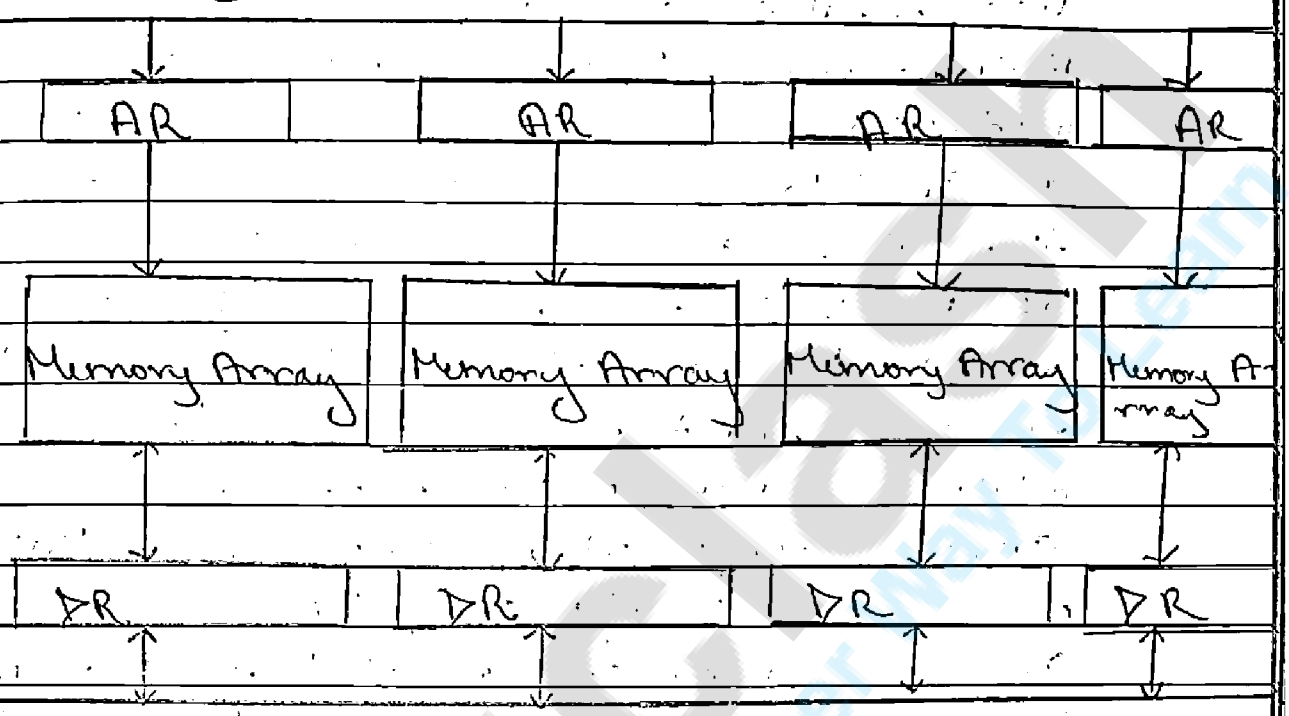
of memory that retains its contents until it is exposed to ultraviolet light. The ultraviolet light clears its contents, making it possible to reprogram the memory. To write to and erase an EPROM, you need a special device called a PROM programmer or PROM burner. However, the constant erasing and rewriting will eventually render the chip useless.

EEPROM :- Short form of Electrically Erasable Programmable Read Only Memory. EEPROM is a special type of PROM that can be erased by exposing it to an electrical charge. Like other types of PROM, EEPROM retains its contents even when the power is turned off. Also like other types of ROM, EEPROM is not as fast as RAM. EEPROMs are used to store a computer system's BIOS and can be updated without returning the unit to the factory. In many cases, BIOS updates can be carried out by computer users using a BIOS update

Q5) Interleaved Memory :- Memory interleaving is the technique used to increase the throughput. Main memory is composed of DRAM memory chips. A number of chips grouped together to form a memory bank. The core idea is to split the memory system into independent banks, which can answer read or write requests independent in parallel. Each bank is independently able to service a memory read and write request, so that a system with K banks can service K request simultaneously, increasing

memory read or write rates by a factor of K. If consecutive words of memory are stored in different banks, then the transfer of block of memory is speeded up.



or

Q6) Associative Memory :- Also called as Content-addressable memory (CAM), associative storage or associative array. Content-addressed or associative memory refers to a memory organization in which the memory is accessed by

its content. It is a special type of computer memory used in certain very high speed searching applications.

In standard computer memory (RAM) the user supplies a memory address and the RAM returns the data word stored in that address.

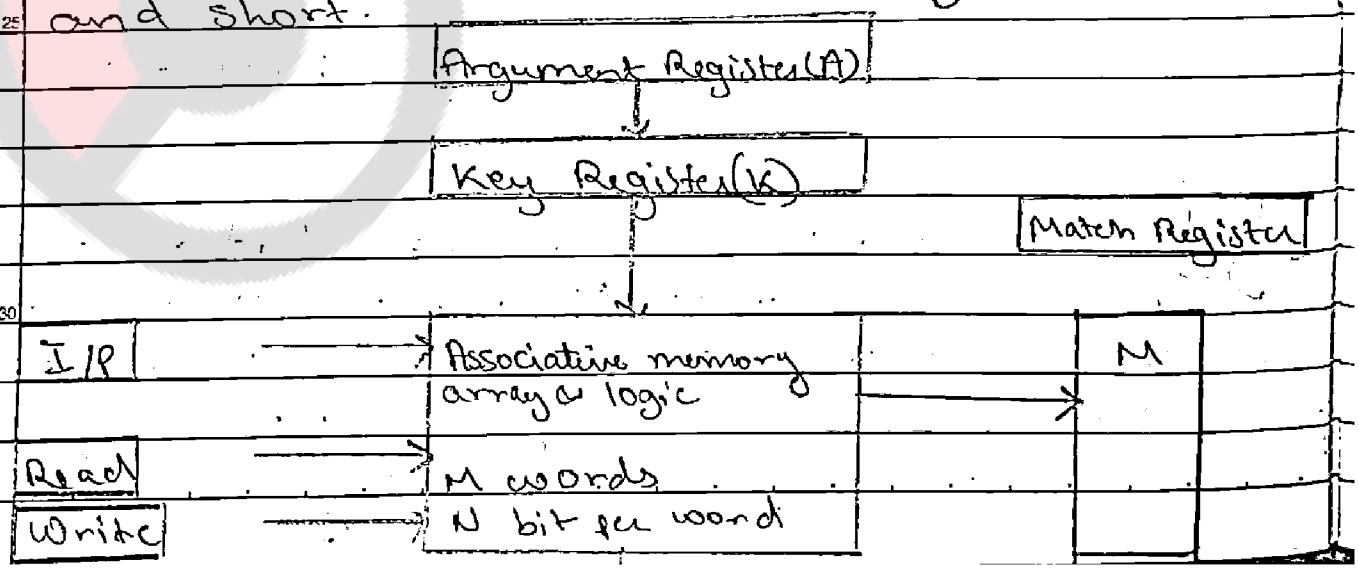
In CAM the user supplies a data word and then CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found.

CAM is designed to search its entire memory in a single operation.

In CAM, each cell must have storage capability as well as logic circuits for matching its content with an external argument.

Associative memories are expensive compared to RAMS because of the added logic associated with each cell. It is much faster than RAM in virtually all search applications.

Associative memories are used in applications where the search time is very critical and short.



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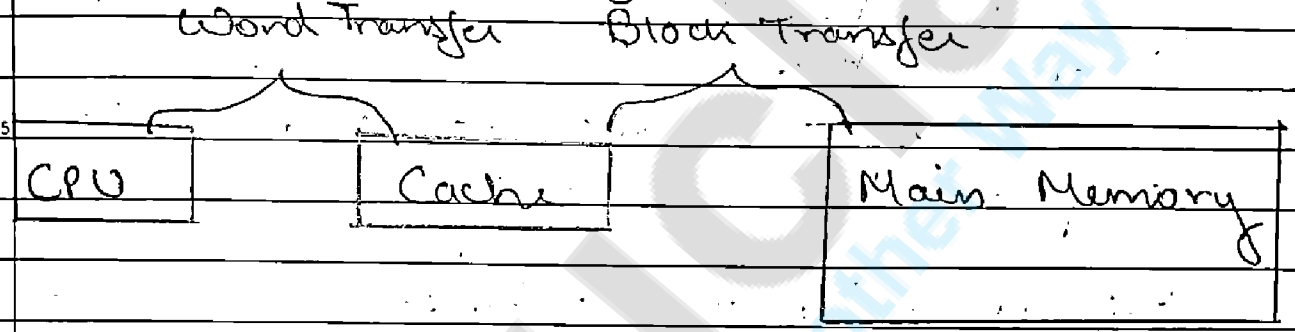
Block Diagram of Associative Memory

Q7) Why Cache memory is needed? Name various elements of cache design. / Explain different types of cache memory mapping techniques in details.

Cache :- • Small amount of fast memory
• Sits between normal main memory and CPU
• May be located on CPU chip or module
• It is relatively expensive



Cache memory is high-speed SRAM ~~that a computer or micro processor can access more quickly that it~~ used to increase the speed of processing by making current programs and data available to CPU at a rapid rate. The purpose of cache memory is to store program instructions and data that are used repeatedly in the operation of programs or information that the CPU is likely to need next.
The computer processor can access this info quickly, from cache memory rather than having it from computers main memory. Fast access to these instructions increases the overall speed of the program.
Cache is used to store segments of programs

currently being executed in CPU & temporary data frequently needed to do calculations.

Elements of Cache design :-

1) Size :- Size of the cache should be small enough so that overall average cost per bit is close to that of main memory alone and large enough so that overall average access time is close to that of the cache alone.

2) larger is cache, larger is the no of gates involved in addressing the cache, as a result performance decreases i.e cache becomes slower.

Cache size also depend on the available chip and board area.

2) Mapping function :- Basic characteristic of cache is its fast access time, so time should not be wasted while searching for words in cache.

There are fewer cache lines than main memory blocks, an algorithm is needed for mapping main memory blocks into cache lines i.e means is needed to determine which main memory blocks occupies a cache line.

The transformation of data from main memory to cache is referred to as a mapping process.

Mapping function determines how the cache is organized.

There are 3 types of mappings :-

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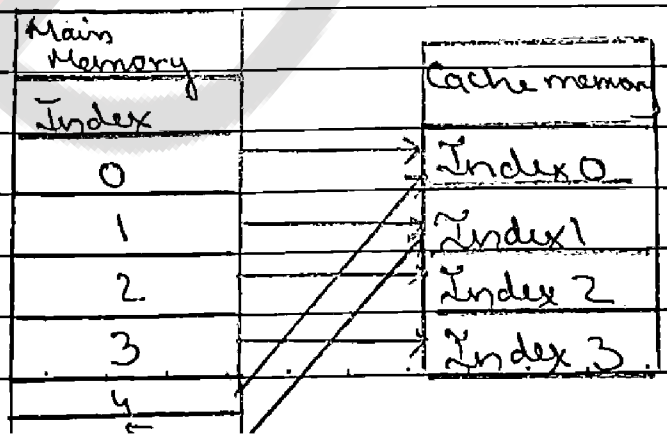
a] Direct Mapping
b] Associative Mapping
c] Set Associative Mapping

a] Direct Mapping :- This is the simplest form of mapping. One block from main memory maps into one possible line of cache memory. As there are more blocks of main memory than there are lines of cache, many blocks in main memory can map to the same line in cache.

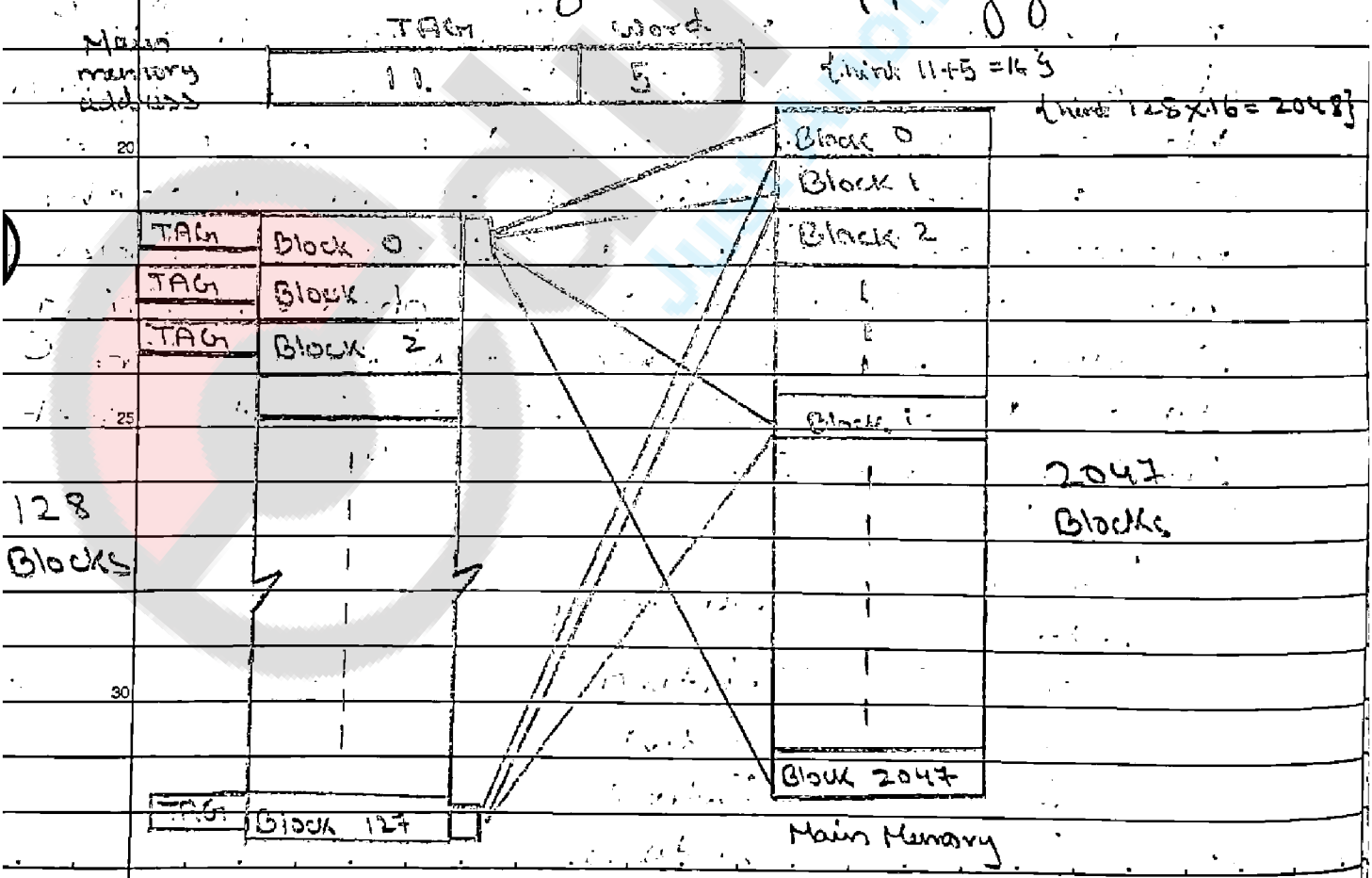
To implement this function, use the formula
$\alpha = \beta \% \gamma$
where α is the cache line number, β is the block number in main memory, γ is the total number of lines in cache memory and % being the modulus operator.

The main disadvantage of using this type of mapping is that there is fixed cache location for any given block in main memory. If two blocks of memory sharing the same cache line are being continually referenced, cache misses would occur and these two blocks would continuously be swapped, resulting in slower memory access due to the time taken to access main memory (or the next level of memory).



b) Associative Mapping - Associative mapping overcomes the disadvantage of direct mapping by permitting each main memory block to be loaded into any line of the cache. In this 12 tag bits are required to identify a memory block when it is present in cache. The tag bits of an address received from processor are compared to the tag bits of each block of the cache to see if the desired block is present.

Cost of an associated mapping cache is higher than the cost of direct-mapped because of the need to search all 128 tag patterns to determine whether a block is in cache also known as associative search. It is considered to be the fastest and the most flexible mapping form.



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c) Set Associative Mapping :- Set associative mapping is introduced to overcome the high conflict miss in the direct mapping technique and the large tag comparisons in case of associative mapping.

In this cache memory mapping technique, the cache blocks are divided into sets. Here the set size is always in the power of 2, i.e if the cache has 2 blocks per set then it is called as 2-way set associative. Similarly, if it has 4 blocks per set then it is called as 4-way set associative.

It basically means that instead of just referring to the cache block directly we will refer to the particular sets present in the cache memory. So basically the concept is we map a particular ~~bo~~ block of main memory to a particular set of cache and within that set, the block can be mapped to any of the cache blocks that are available.

Consider a system with 128 cache memory blocks and 4096 primary memory blocks. Here we are considering 2 blocks in each set, or simply we are considering a 2-way set associative process. Since there are 2 blocks in each set, so there will be total 64 sets in our cache memory.

128×32 = 4096

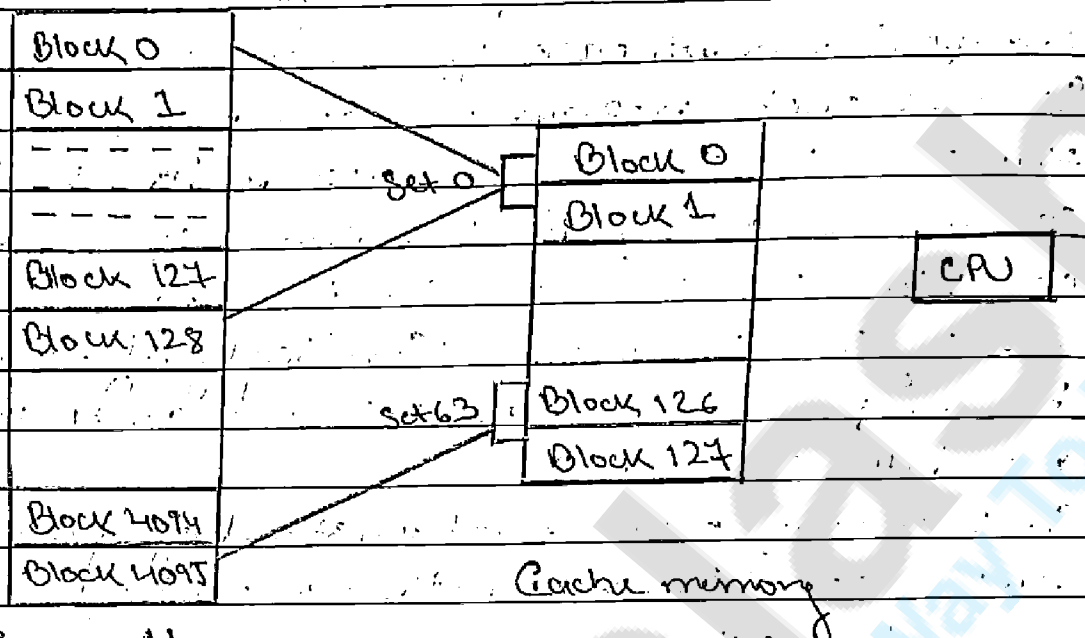
32×2=64

Here, to determine the proper set position in which the main memory will be placed we use a concept i.e if the ith block of main memory has to be placed in the jth block of cache memory then,

$$j = i \% (\text{number of sets in cache})$$

After determining the cache position the primary memory block may be placed in any

block inside the set. Following diagram illustrates this process



3) Replacement Algorithms :- Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced. For direct mapping where there is only one possible line for a block of memory, no replacement algorithm is needed. For associative and set associative mapping, however an algorithm is needed. For maximum speed, this algorithm is implemented in the hardware. Four of the most common algorithms are:-

a) Least Recently Used (LRU):- This cache algorithm keep recently used items near the top of cache. Whenever a new item is accessed, the LRU places it at the top of the cache. When the cache limit has been reached, items that have been accessed less recently will be removed.

starting from the bottom of the cache. This can be an expensive algorithm to use, as it needs to keep "age bits" that show exactly when the item was accessed. In addition, when a LRU cache algorithm deletes an item, the "age bit" changes on all the other items.

b) Least Frequently Used (LFU) :- This cache algorithm uses a counter to keep track of how often an entry is accessed. With the LFU cache algorithm, the entry with the lowest count is removed first. This method isn't used that ~~often~~ often, as it does not account for an item that has an initially high access rate and then was not accessed for a long time.

c) First In First Out :- This replaces the candidate line in the cache that has been there in the longest.

d) Random replacement :- ~~This~~ The simplest algorithm is to choose the block to be overwritten at random. ~~Its~~ Interestingly enough, this simple algorithm has been found to be very effective in practice.

4) Write Policy :- In addition to caching reads from memory, the system is capable of caching writes to memory. The handling of the address bits and the cache lines, etc is pretty similar to how this is done when the cache is read. However, there are two different ways that the cache handles writes, and is referred to as the "write policy" of the cache.

Write-Through Policy :- One of the central

caching policies is known as write-through. This means that data is stored and written into the cache and to the primary storage ~~device~~ device at the same time. One advantage of this policy is that it ensures information will be stored safely without risk of data loss. If the computer crashes or the power goes out, data can still be recovered without issue. To keep data safe, this policy has to perform every write operation twice. The program or application that is being used must wait until the data has been written to both the cache and storage device before it can proceed. This comes at the cost of system performance but is highly recommended for sensitive data that cannot be lost. Many business that deal with sensitive customer information such as payment details would most likely choose this method since that data is very critical to keep intact.

Write-Back Policy:- The other well-known caching policy is called write-back. This method saves data only to the cache when processing. It is important to note that there are only certain times or conditions where the information will also be written to the primary storage device as well. Since there is no guaranteed way to keep the data safe, this policy has a much higher probability of data loss if ~~if~~ something were to go wrong. At the same time, since it no longer

has to write information to both cache and storage device, system performance gains are noticeable when compared to the write-through policy. Data recoverability is exchanged for system performance, making this ideal for applications or programs that require low latency and high ~~performance~~ throughput. The write-back policy would be a good fit to use with less sensitive data where the occasional loss would be considered acceptable.

5) Line Size :- Larger blocks reduces the number of blocks that fit into a cache. Because ~~that~~ each block fetch overwrites older cache contents, a small number of block results in data being overwritten shortly after they are fetched.
As a block becomes larger, each additional word is ~~farther~~ farther from the requested word and therefore less likely to be needed in the near future.

6) No of Caches :- When caches were originally introduced, the typical system had a single cache. More recently, the use of multiple caches has become an important aspect. There are two design issues surrounding number of caches.

a) MULTILEVEL CACHES :- Most contemporary designs include both on-chip and external caches. The simplest such ~~design~~ organization is known as a two-level

cache, with the internal cache designated as level 1 (L1) and the external cache designated as level 2 (L2). There can also be 3 or more levels of cache. This helps in reducing main memory accesses.

b) UNIFIED VERSUS SPLIT CACHES :- Earlier on-chip cache designs consisted of a single cache used to store references to both data and instructions. This is the unified approach. ~~Mos~~ More recently, it has become common to split the cache into two: one dedicated to instructions and one dedicated to data. These two caches both exist at the same level. This is the split cache. Using a unified cache or a split cache is another design issue.

Q8) RAID and its levels :- RAID is an acronym for Redundant Array of Independent Disks. In fact, RAID is the way of combining several independent and relatively small disks into a single storage of a large size. The disks included into the array are called array members. The disks can be combined into the array in different ways which are known as RAID levels. Each of RAID levels has its own characteristics of :-

• Fault-tolerance :- which is the ability to ~~survive~~ survive of one or several disk failures.

• Performance :- which shows the change in the read and write speed of the entire array as compared to a single disk.

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• The capacity of the array which is determined by the amount of user data that can be written to the array. The array capacity depends on the RAID level and does not always match the sum of the sizes of the RAID number disks.

RAID Storage techniques

The main methods of storing data in the array are:

• Striping :- splitting the flow of data into blocks of a certain size (called "block size") then writing of these blocks across the RAID one by one. This way of data storage affects on the performance.

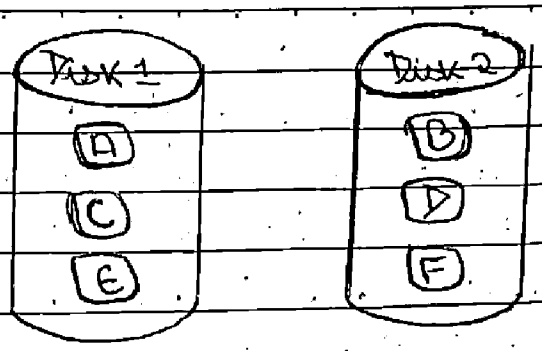
• Mirroring :- is a storage technique in which the identical copies of data are stored on the RAID members simultaneously. This type of data placement affects the fault tolerance as well as the performance.

• Parity is a storage technique which is utilized striping and checksum methods. In parity technique, a certain parity function is calculated for the data blocks. If a drive fails, the missing blocks are recalculated from the checksum, providing the RAID fault tolerance.

All the existing RAID types are based on striping, mirroring, parity or combination of these storage techniques.

RAID levels

1) RAID 0 :-

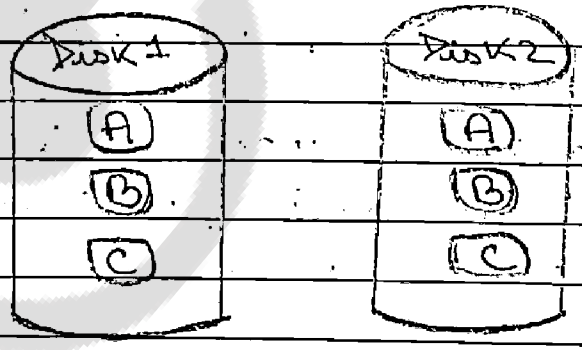


Blocks Striped. No Mirror. No Parity

1) Minimum 2 disks.
2) Excellent performance (as blocks are striped)
3) No redundancy (no mirror; no parity).
4) Very simple design
5) Easy to implement
6) Don't use this for any critical system.

Applications:
1) Video Production and Editing
2) Image Editing
3) Any application requiring high bandwidth
4) Live streaming

2) RAID 1 :-



Blocks mirrored. No stripe. No parity

1) Minimum 2 disks
2) Good performance (no striping, no parity).
3) Excellent redundancy (as blocks are

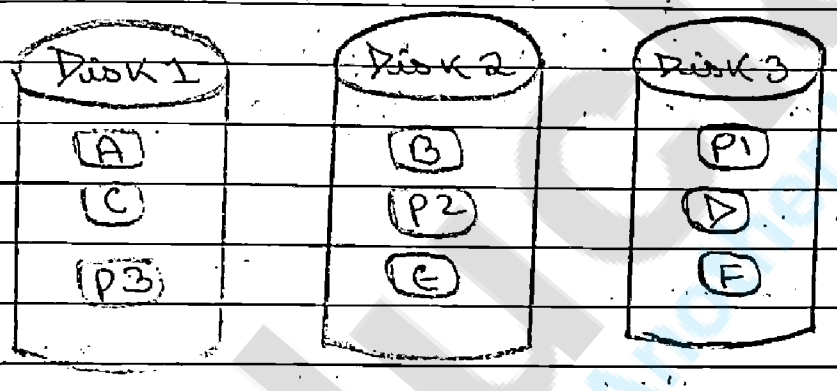
mirrored).

4) Recovery from a failure is simple. When a drive fails, the data may still be accessed from second drive

Applications:-

1) Accounting
2) Payroll
3) Financial
4) Any application requiring very high availability

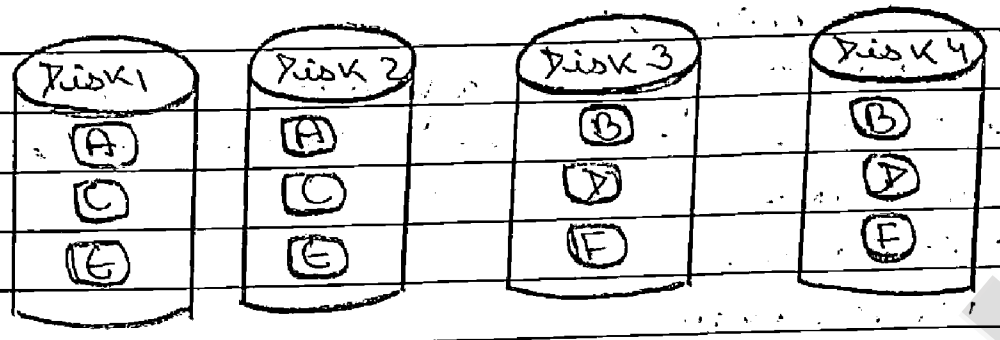
3) RAID 5



Blocks striped. Distributed Parity

1) Minimum 3 disks
2) Good performance (as blocks are striped).
3) Good redundancy (distributed parity)
4) Best cost effective option providing both performance and redundancy. Use this for DB that is heavily read oriented. Write operations will be slow.

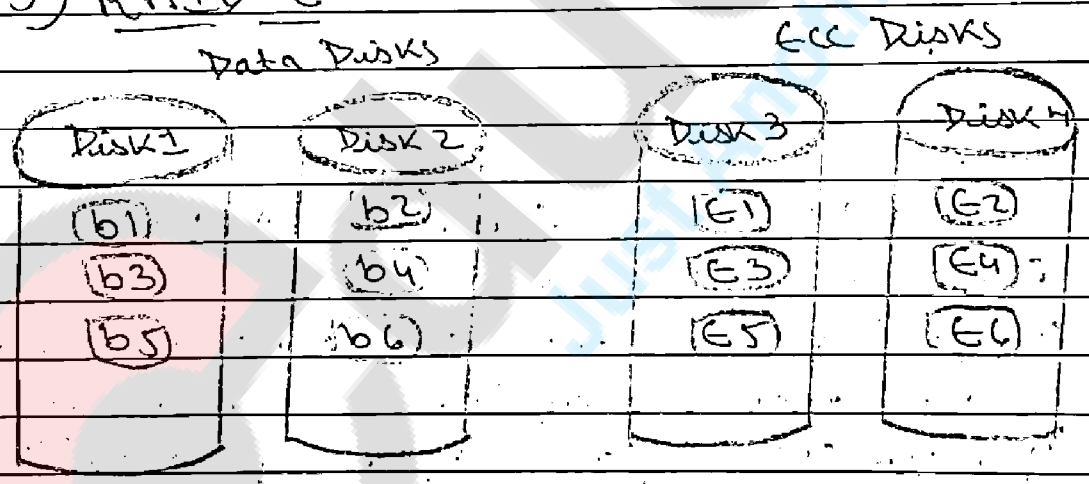
4) RAID 10



Blocks Mirrored (and Blocks Striped)

1) Minimum 4 disks
2) This is also called as "stripe of mirrors"
3) Excellent redundancy (as blocks are mirrored)
4) Excellent performance (as blocks are striped)
5) This is the best option for any mission critical applications (especially databases).

5) RAID 2



Bits Striped (and stores ECC)

1) This uses bit level striping i.e instead of striping the blocks across the disks, it stripes the bits across the disks.
2) In the above diagram b1, b2, b3 are bits. E1, E2, E3 are error correction codes.
3) You need two groups of disks. One

group of disks are used to write the data, another group is used to write the error correction codes.

4) This uses Hamming error correction code (ECC), and stores this information in the redundancy disks.

5) When data is written to the disks, it calculates the ECC code for the data on the fly; and stripes the data bits to the data-disks and writes the ECC code to the redundancy disks.

6) When data is read from the disks, it also reads the corresponding ECC code from the redundancy disks and checks whether the data is consistent. If required, it makes appropriate corrections on the fly.

7) This uses lot of disks and can be configured in different disk configuration.

8) This is not used anymore. This is expensive and implementing it in a RAID controller is complex and ECC is redundant now-a-days as the hard disk themselves can do this.

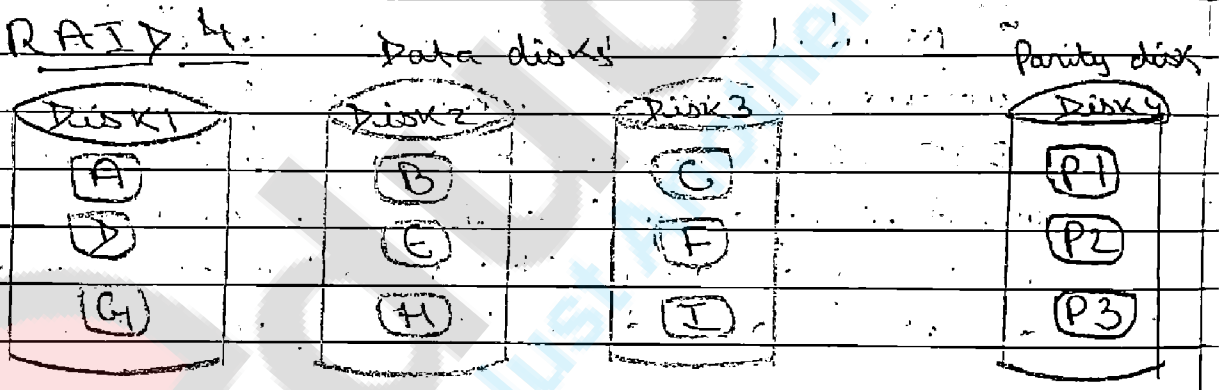
6) RAID 3 :-

Data disks			Parity Disk
Disk 1	Disk 2	Disk 3	Disk 4
B1	B2	B3	P1
B4	B5	B6	P2
B7	B8	B9	P3

Bytes Striped (and dedicated Parity Disk)

1) This uses byte level striping i.e instead of striping the blocks across the disks, it stripes the bytes across the disks.
2) In the above diagram B1, B2, B3 are bytes. P1, P2, P3 are parities.
3) Uses multiple data disks and a dedicated disk to store parity.
4) The disks have to spin in sync to get to the data.
5) Sequential read and write will have good performance.
6) Random read and write will have worst performance.
7) This is not commonly used.

7) RAID 4.

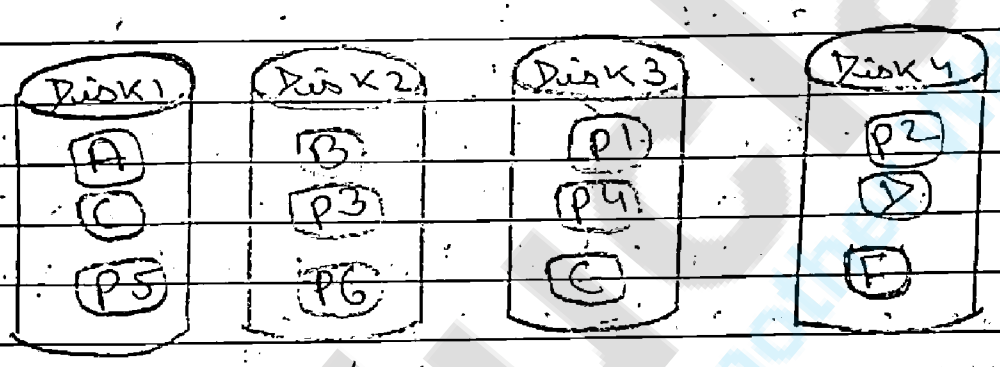


Block striped and dedicated parity disk

1) This uses block level striping
2) In the above diagram A, B, C are blocks. P1, P2, P3 are parities.
3) Uses multiple data disks and a dedicated disk to store parity.
4) Minimum of 3 disks (2 disks for data and 1 for parity)
5) Good random reads, as the data blocks are striped.

6) Bad random writes as for every write, it has to write to the single parity disk.
7) It is somewhat similar to RAID 3 and 5, but a little different.
8) This is just like RAID 3 in having the dedicated parity disk but this stripes blocks.
9) This is just like RAID 5 in striping the blocks across the data disks, but this has only one parity disk.
10) This is not commonly used.

8) RAID 6



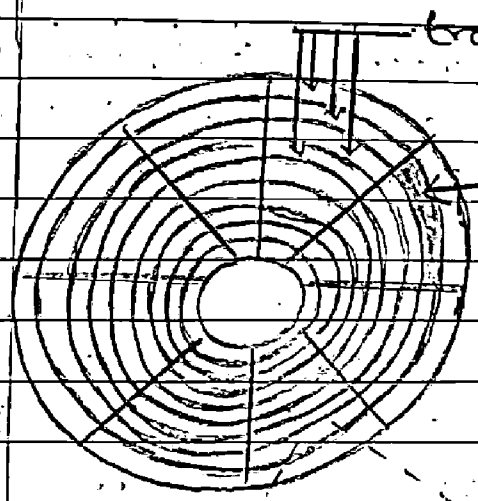
Blocks Striped · Two distributed Parity

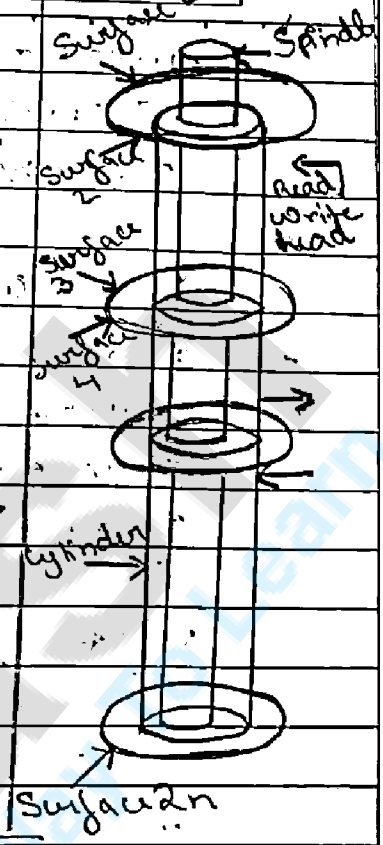
1) Just like RAID 5, this does block level striping. However, it uses dual parity.
2) In the above diagram A, B, C are blocks. P1, P2, P3 are parities
3) This creates two parity blocks for each data block.
4) Can handle two disk failure.
5) This RAID configuration is complex to implement in a RAID controller, as it has to calculate two parity data for each data block.

Q9) Magnetic Disk:- In modern computers, Magnetic Disk is used for secondary storage. Like Magnetic tape, the magnetic disk is also a non-volatile so, ~~as~~ it stores the data permanently. The magnetic disk has a several flat circular shaped platters which appear like a CD. Both inner and outer surfaces of the platter are covered with the magnetic material so that information can be recorded magnetically on the platters. There is a read-write head that moves over the surface of each platter. These read-write heads are attached to the disk arm that helps in moving all heads as a single unit.

Each platter surface is divided into circular tracks which are further divided into sectors. The read-write head flies over the platter surface on a thin cushion of air. Though the disk platter is coated with a protective layer, there is always a danger that head will make contact with the disk causing head crash. The head crash is not repairable, the whole magnetic disk is to be replaced.

Magnetic disk is fast in accessing data sequentially or randomly compared to magnetic tape which allows fast sequential accessing but ~~is~~ is slower in random accessing.





Q10) Optical Memory :- It is called optical memory because the read/write operation is done with help of laser diode which is an optical device. Besides their ability to store large amount of data, optical disks have the advantage that they are relatively inexpensive and immune to dust, and most are removable. Also, since the data is written on the disk and read off the disk with the light from tiny laser diode, the read/write head does not have to touch the disk, so that the read/write head will not crash on small dust particles and destroy the recorded data as it can with magnetic hard disks.

Some optical disk systems record data in concentric circular tracks as magnetic disks do. Other such as CD systems record data on single spiral track.

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Types of Optical Memories :- 1) Read Only
2) Write Once | Read Many (WORM)
3) Erasable Optical Or Read / Write

Read only Optical Memory :- Read only systems allow prerecorded disks to be read out. A disk which can only be read from is often called an optical ROM or OROM. Example is an pre-recorded audio CD.

WORM :- These systems allow you to write data on the disks, but once the data is written on to the disk, it can not be erased or changed.
The stored data can be read out as many times as ~~disc~~ disired.

Erasable Optical Disks :- Erasable optical or EO systems allow you to erase recorded data and write new data on to the disk. The recording materials and recording methods are different for these different types of systems.

Examples of Optical Memory :-

CD-ROM : CD ROM or Compact-Disk Read Only Memory are optical storage device which can be easily read by computer but ~~or~~ not written. CD-ROMs are stamped by the vendor, and once stamped, they cannot be erased and filled with new data. To read a CD, CD-ROM player is.

needed. All CD-ROMs conform to a standard size and format, so any type of CD-ROM can be loaded into any CD-ROM player. In addition, CD-ROM players are capable of playing audio CDs, which share same technology. CD-ROMs are particularly well-suited to information that requires large storage capacity. This includes large software applications that support colour, graphics, sound and especially video.

Advantages :- 1) Storage capacity is high
2) Data storage cost per bit is reasonable
3) Easy to carry.
4) Can store variety of data.

Disadvantages :- 1) CD-ROMs are read only.
2) Access time is more than hard disk.

DVD-ROM, DVD-R and DVD-RAM :- DVD or Digital Versatile Disk is another form of optical storage. These are higher in capacity than the CDs. Pre-recorded DVDs are mass-produced using molding machines that physically stamp data onto the DVD. Such disks are known as DVD-ROM, because data can only be read and not written nor erased. DVD Rs are the blank record able DVDs which can be recorded once using optical disk recording technologies by using DVD recorders and then function as a DVD-ROM. ~~DVD-ROM~~ Re writable DVDs DVD-RAM can be recorded and erased multiple times.

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Q.11) Flash Memory :- A special type of memory that works like both RAM and ROM. You can write information to flash memory like you can with RAM, but the information ~~was~~ isn't erased when the power is off, like it is with ROM.

Flash memory is a type of Electronically Erasable Programmable Read-Only Memory memory chips that retain information without requiring power. Regular EEPROM erased content byte by byte; most flash memory erases data in whole blocks, making it suitable for use with applications where large amounts of data require frequent updates. Inside the flash chip, data is stored in cells protected by floating gates. Tunneling electrons change the ~~gates~~ gate's electronic charge in "a flash" (hence the name), clearing the cell of its contents so it can be rewritten.

Flash memory devices use two different logical technologies - NOR and NAND to map data. NOR flash provides high-speed random access, reading and writing data in specific memory locations; it can retrieve as little as a single byte. NOR is used to store cell phones operating systems; its also used in computers for the BIOS program that run's at start-up.

NAND flash reads and writes sequentially at high speed, handling data in small blocks called pages. This flash is used in solid-state and USB flash drives,

digital cameras, audio and video players and TV set-up boxes. NAND flash reads faster that it writes, quickly transferring whole pages of data. Less expensive than NOR flash, NAND technology offers higher capacity for the same-size silicon.

As a NAND chip wears out, erase/program operations slow down considerably, causing more retries and bad block remapping. Moving many small files could further degrade transfer rates. Catastrophic failure happens only with extended use (after thousands of writes and accesses); periodic backup and replacement forestall this problem.

Flash Applications :- USB, Memory Cards, Solid-state drives

Q12) Virtual Memory :- is the feature of an operating system (O.S). It is responsible for memory management. In the Virtual Memory the Physical Memory (Hard Disk) will be treated as the logical Memory (RAM). Means with the help of virtual memory we can also temporarily increase the size of logical Memory as from the Physical Memory. A user will see or feels that all the programs are running into the logical Memory of the computer. With the help of virtual memory all the space of hard disk can be used as the logical memory so that a user can execute any number of programs.

Benefits of Virtual Memory

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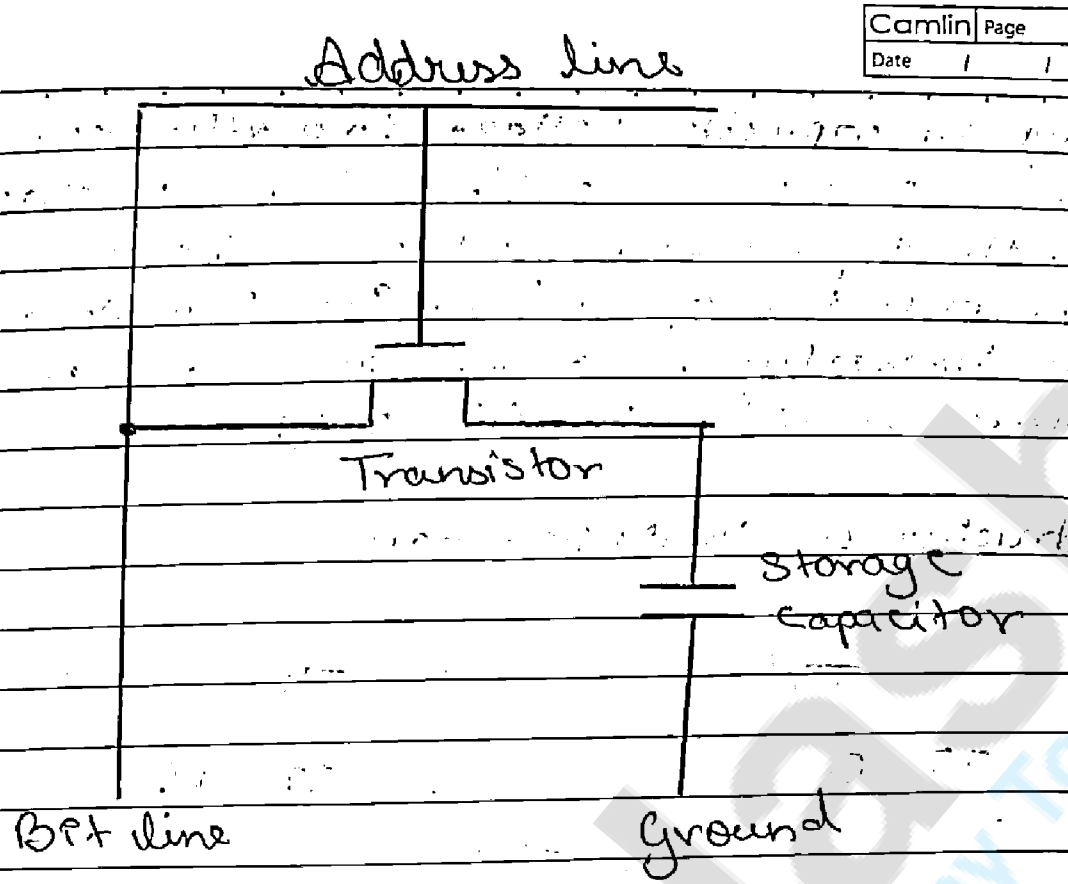
1) Unused Address space :- With the help of Unused Address space a user can execute any number of programs because all the actual addresses will be treated as the logical addresses. All the programs those are given by the user will be stored into the disk space and all the programs will be stored into the physical address space but they will treat as they are stored into the logical address space.

2) Increased degree of Multiprogramming :- With the help of Virtual Memory we can execute many programs at a time because many programs can be fit in the physical memory so that more programs can be stored into the memory but this will not increase the response time of the CPU means this will not affect on the execution of the program.

3) Decrease Number of I/O operations :- There will be less operations those are to be used for performing the swapping of the processes. All the programs will be automatically loaded into the memory when they are needed.

But always remember that the whole programs are never to be copied into the memory means all the programs will be copied into the form of pages i.e the parts of the programs.

Q3] Structure of DRAM



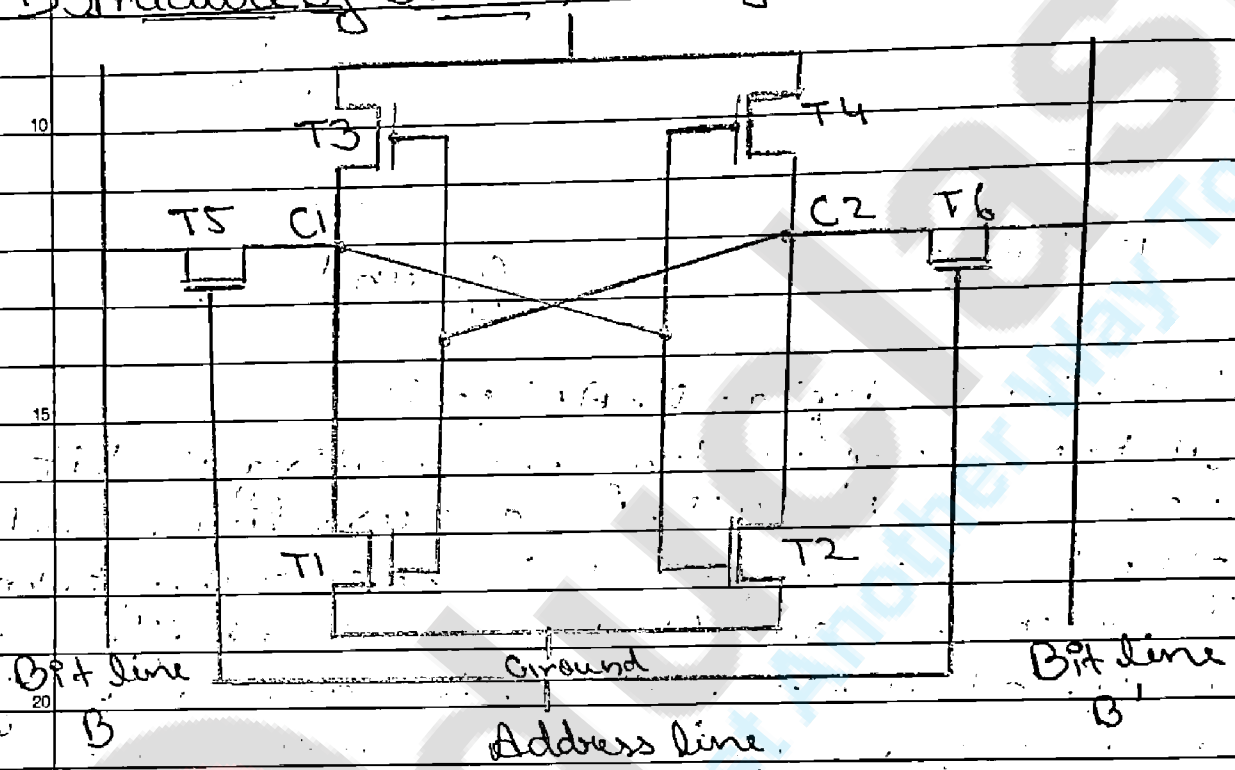
Working of typical DRAM cell:-

At the time of reading and writing the bit value from the cell, the address line is activated. The transistor present in the circuitry ~~behaves~~ behaves as a switch that is closed if voltage is applied to the address line and open if no voltage is applied to the address line. For the write operation, a voltage signal is employed to the bit line where high voltage shows 1 and low voltage indicates 0. A signal is then used to the address line which enables transferring of the charge to the capacitor.

When the address line is chosen for executing read operation, the transistor turns on and the charge stored on the capacitor is supplied out onto a bit line and to a sense amplifier. The sense amplifier specifies whether the cell contains a logic 1 or logic 2 by compar-

ing the capacitor voltage to a reference value. The reading of the cell results in discharging of the capacitor, which must be restored to complete the operation. Even though a DRAM is basically an analog device and used to store the single bit (i.e 0, 1).

Q14) Structure of SRAM DC voltage



To generate stable logic state, four transistors (T1, T2, T3, T4) are organized in a cross-connected way. For generating logic state 1, node C1 is high and C2 is low, in this state T1 and T4 are off and T2 and T3 are on. For logic state 0, junction C1 is low and C2 is high, in the given state T1 and T4 are on and T2 and T3 are off. Both states are stable until the direct current (dc) voltage is applied.

The SRAM address line is operated for opening and closing the switch and to control the T5 and T6 transistors permitting to read

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and write. For read operation the signal is applied to these address line then T5 and T6 gets on and the bit value is read from line B. For the write operation, the signal is employed to B bit line and its complement is applied to B'.