(3 Hours) **[Total Marks : 80]**

N.B. : 1) Question No.1 is **compulsory.**
2) Attempt any **three** from the remaining five questions.
3) Answer to sub-questions should be grouped together.

Q1. (a) What are multiplexers? Devise a 4:1 multiplexer using basic gates. (05)

(b) Discuss the role of MAR and MBR in instruction execution. (05)

(c) Simplify the circuit represented by the following expression using (10)
Karnaugh's Map
$F(A, B, C, D)=\Sigma(1,3,7,8,10,12,14)+d(0,2,5)$

(d) Discuss the working of R-S Flip flop. (05)

Q2. (a) What are cache memories? Explain the organisation of cache memory in detail. (10)

(b) Discuss the basic functions of a Control Unit. Explain the organisation of a control unit with its block diagram. (10)

Q3. (a) What is instruction pipelining? Explain the six stage Instruction pipelining with an example. Comment on how are branches handled. (10)

(b) Explain the organisation of an I/O module. Discuss the Interrupt Driven I/O and DMA techniques. (10)

Q4. (a) What are RAID? Explain all RAID levels with appropriate diagrams. List the advantages and disadvantages of each RAID level. (10)

(b) Discuss various addressing modes used in instruction design. Give relevant examples of each. (10)

Q5. (a) What is a Bus? Explain various bus interconnection structures. (10)

(b) Discuss memory hierarchy in brief. Explain in detail the structure and working of SRAM. (10)

Q6. Write short notes on **any four** of the following (20)

(a) Primary Counters

(b) Flynn's Taxonomy

(c) CISC

(d) Full Adder

(e) Instruction Cycle State Diagram.
